

MSI:MS-7245 NEC:(Babel)(MT3H)

Version 1.0

System Chipset:

Intel Broadwater - GMCH (North Bridge)

Intel ICH8(DO)(R) (South Bridge)

On Board Chipset:

BIOS -- SPI Flash 8Mb or 16Mb

HD AUDIO -- ALC262

LPC Super I/O -- SMSC--SHC5017

LAN -- Intel Neneveh 82566 DM/DC

IDE-- VIA VT-6410

CLOCK -- CY505YC64CT

Main Memory:

2 CHANNEL DDR II * 4 (Max 8GB)

Expansion Slots:

PCIE x16 SLOT * 1

PCIE x1 SLOT * 1

PCI SLOT * 1

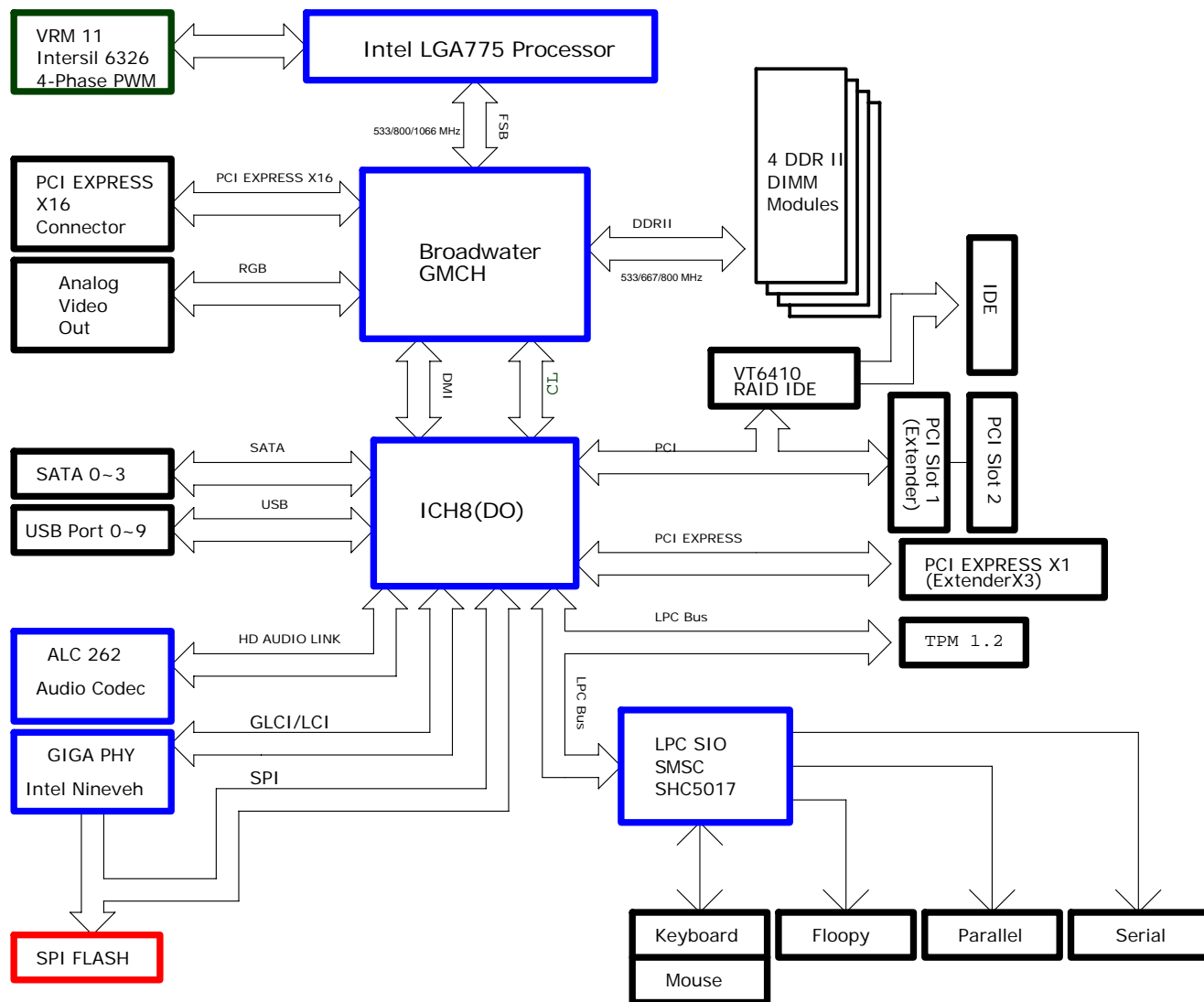
PCI(Extender)SLOT * 1

Intersil PWM:

Controller: INTERSIL 6326 4 PHASES

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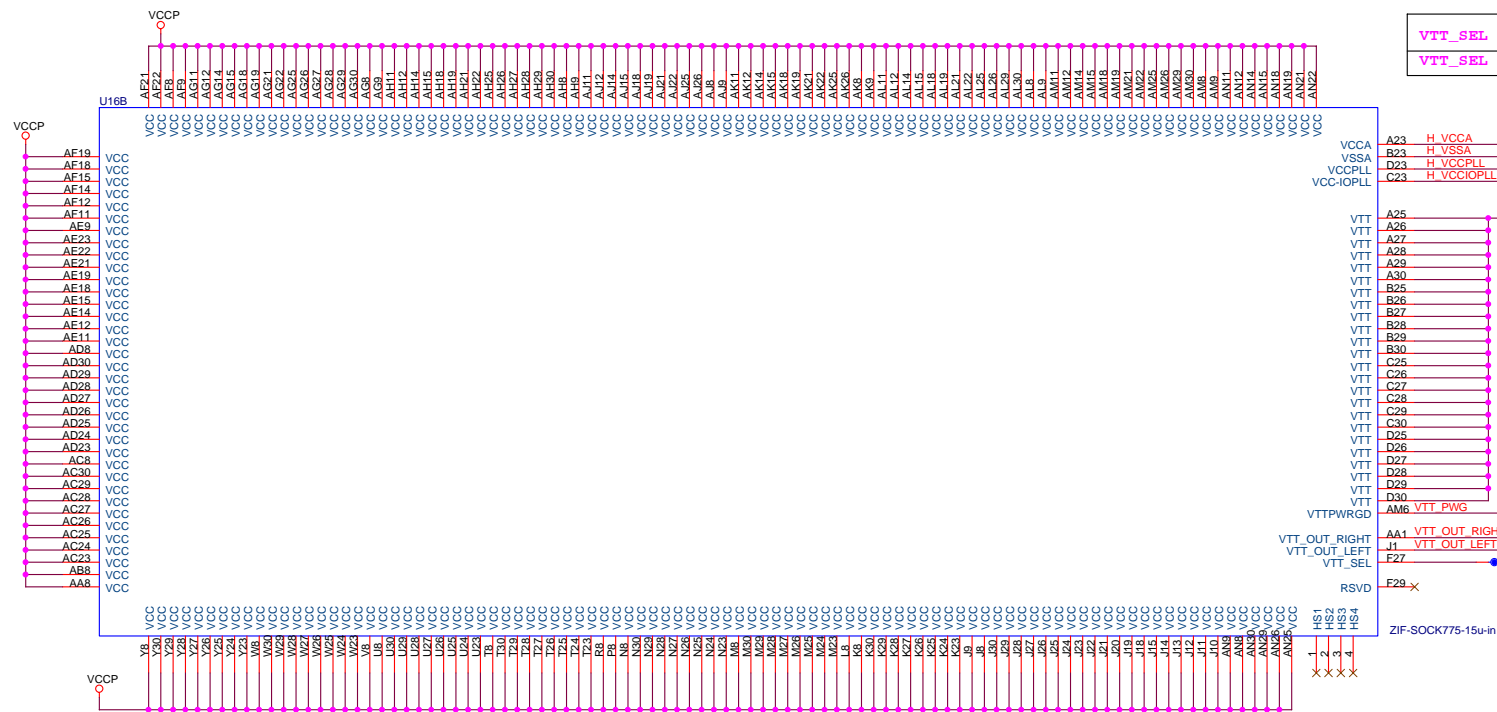
Block Diagram



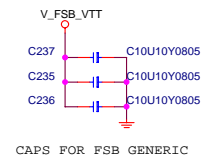
[illegible]

BSEL			TABLE
2	1	0	FSB FREQUENCY
0	0	0	267 MHZ (1067)
0	1	0	200 MHZ (800)
0	0	1	133 MHZ (533)

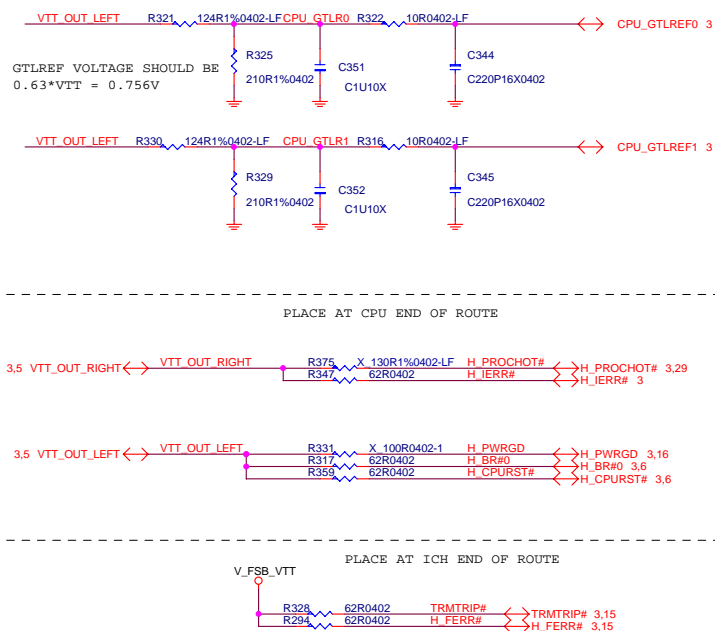
CPU_TMPA_AR75 X 0R0402 ↔ CPU_TMPA_SST 16
VTIN_GND_C X R78 X 0R0402 ↔ VTIN_GND_SST 16
CPU_TMPA_AR76 0R0402 ↔ CPU_TMPA 24
VTIN_GND_C R79 0R0402 ↔ VTIN_GND 24



VTT_SEL = H	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = L	V_FSB_VTT=1.2V	For normal processors.

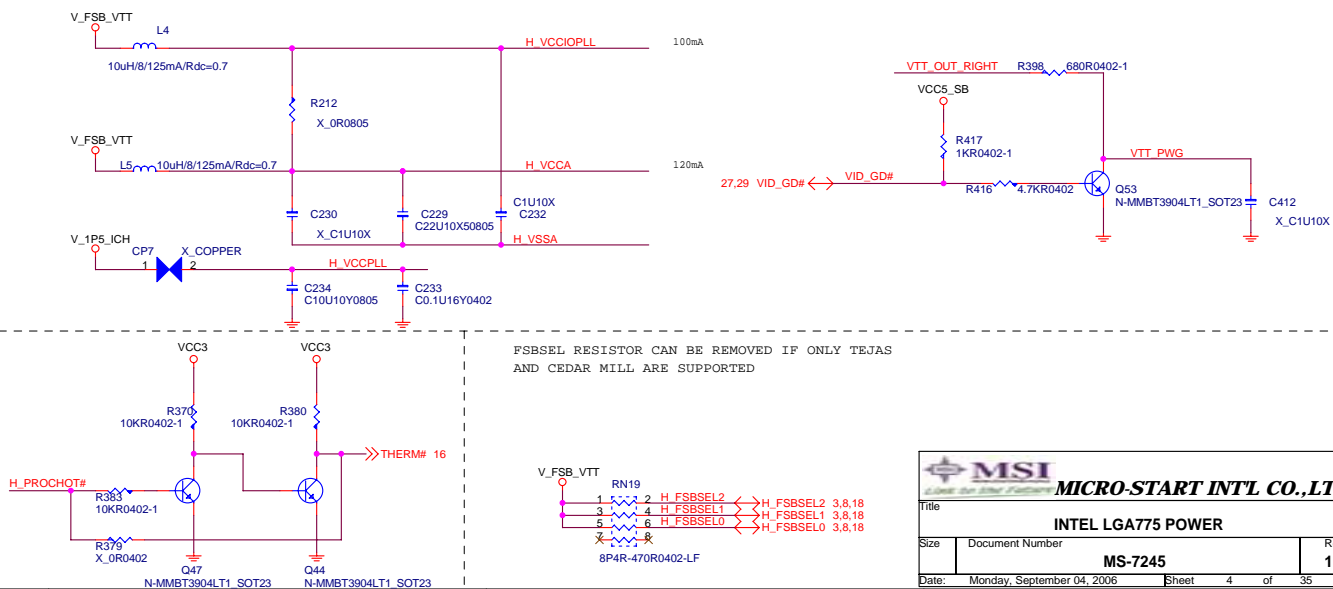


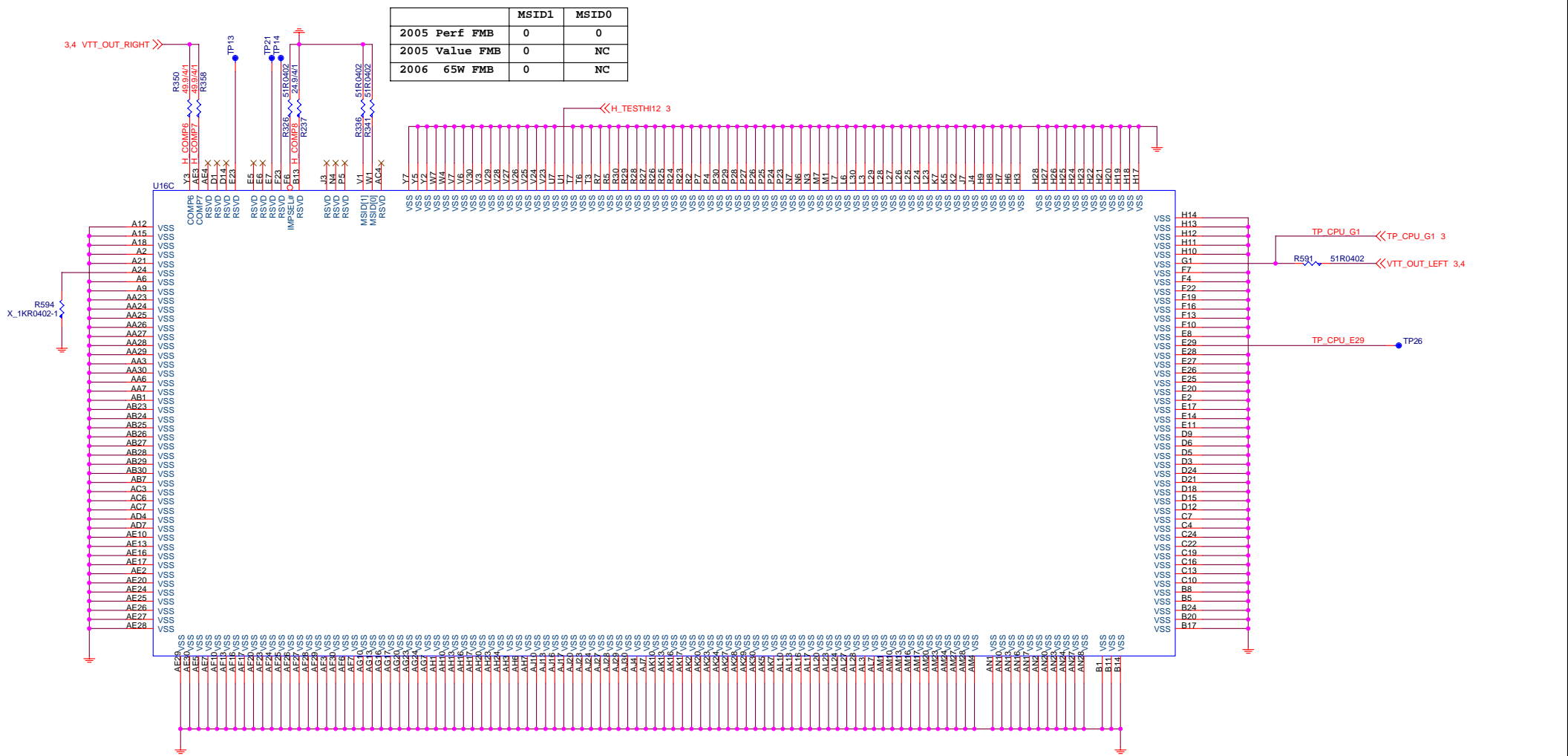
LGA775 pin AM6 is VTT_PWRGD, But for Conroe, AM6 is a reserved pin.(VTT_PWRGD didn't exist on Conroe.)



PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS

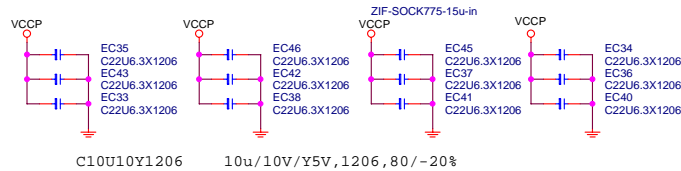
VTT_PWG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns





	MSID1	MSID0
2005 Perf FMB	0	0
2005 Value FMB	0	NC
2006 65W FMB	0	NC

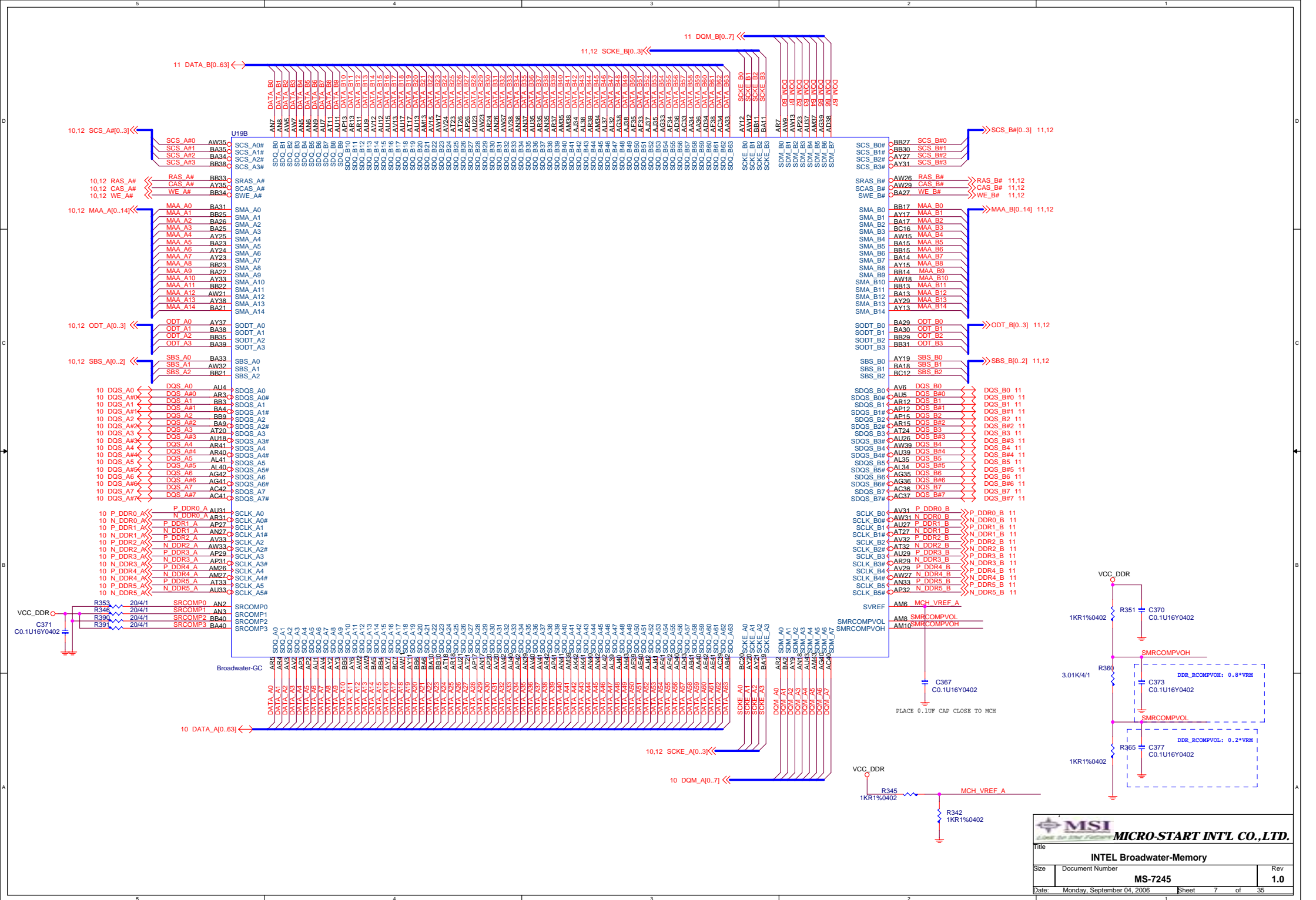
CPU DECOUPLING CAPACITORS

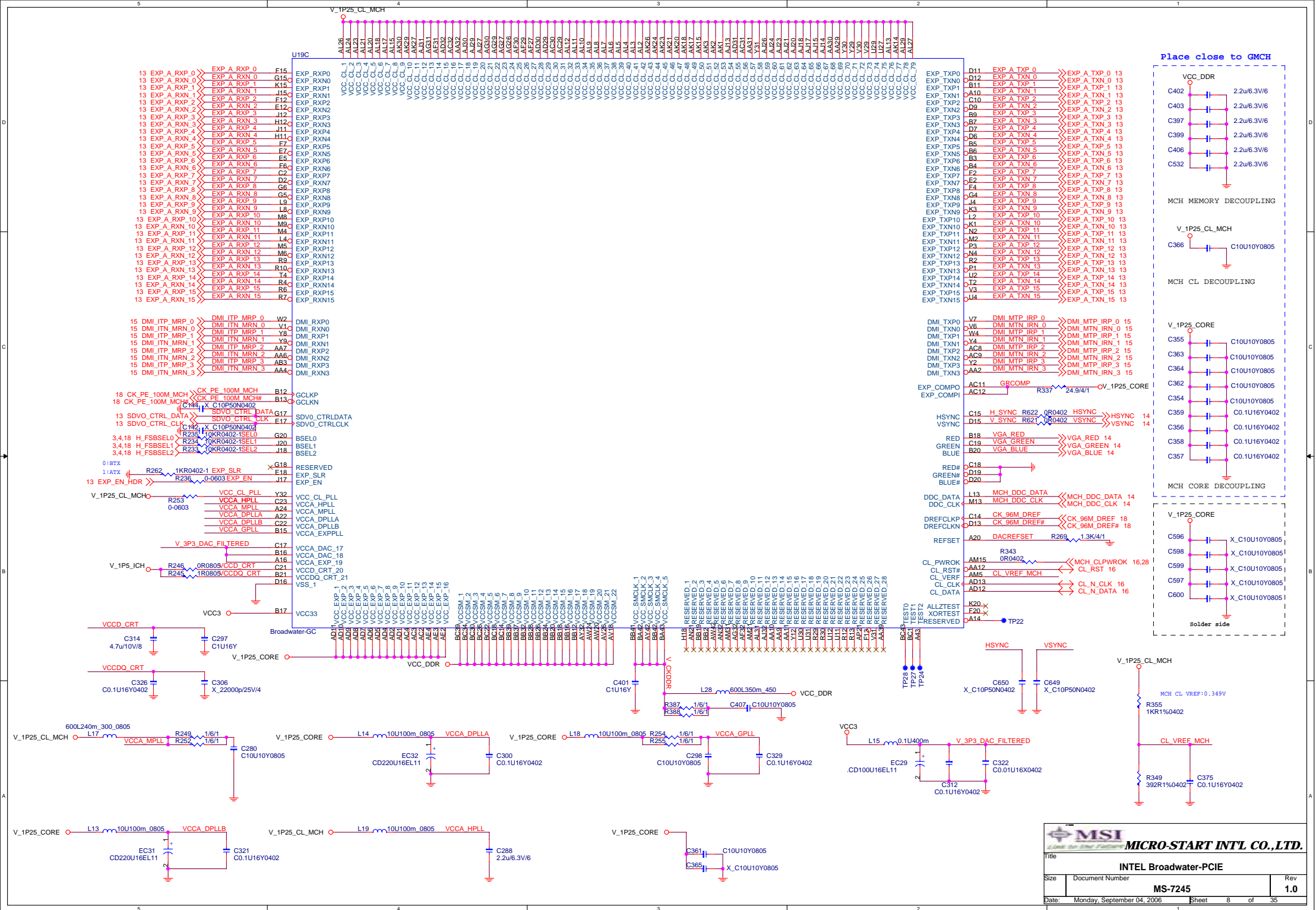


C10U10Y1206

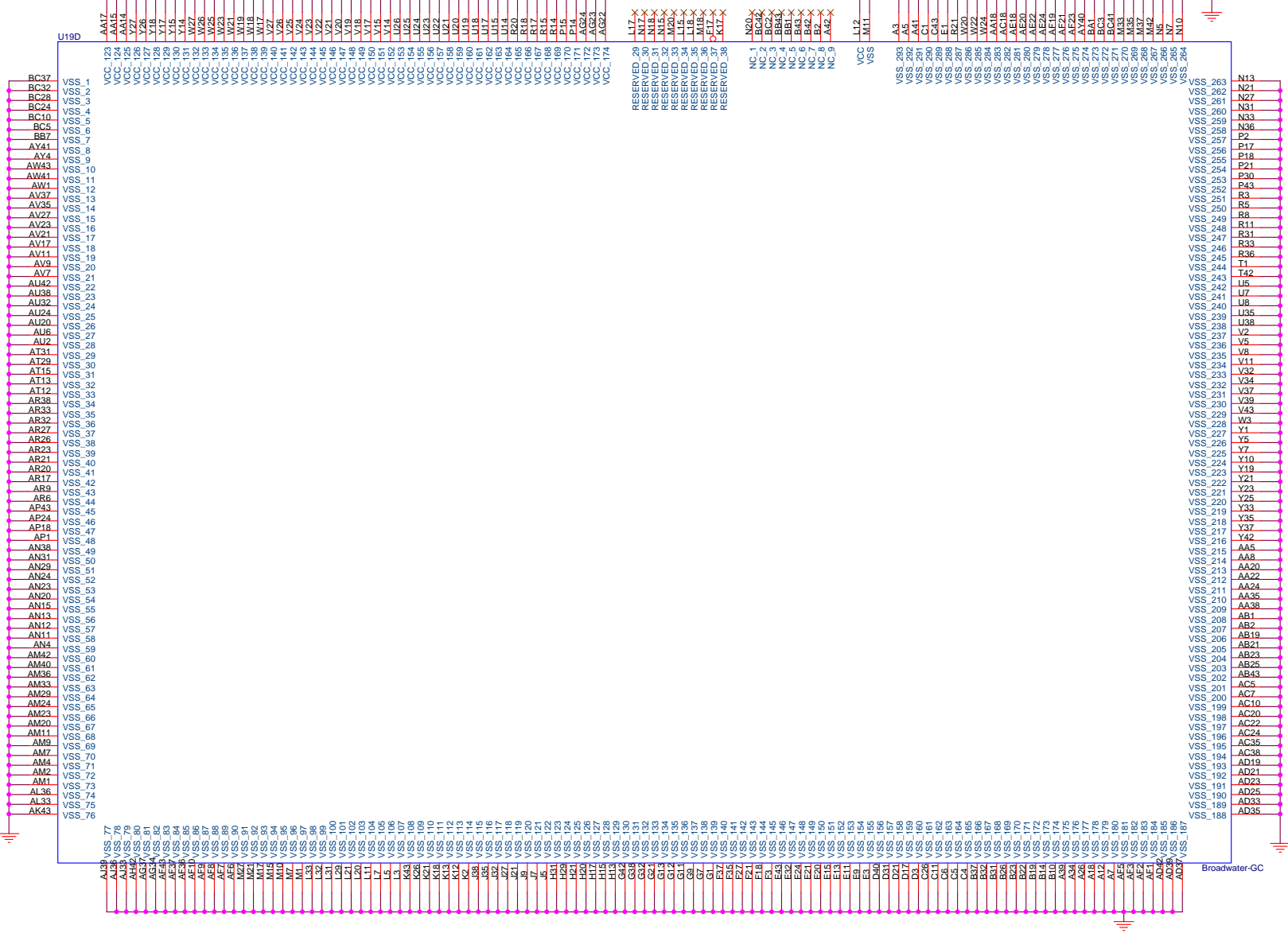
10u/10V/Y5V,1206,80/-20%

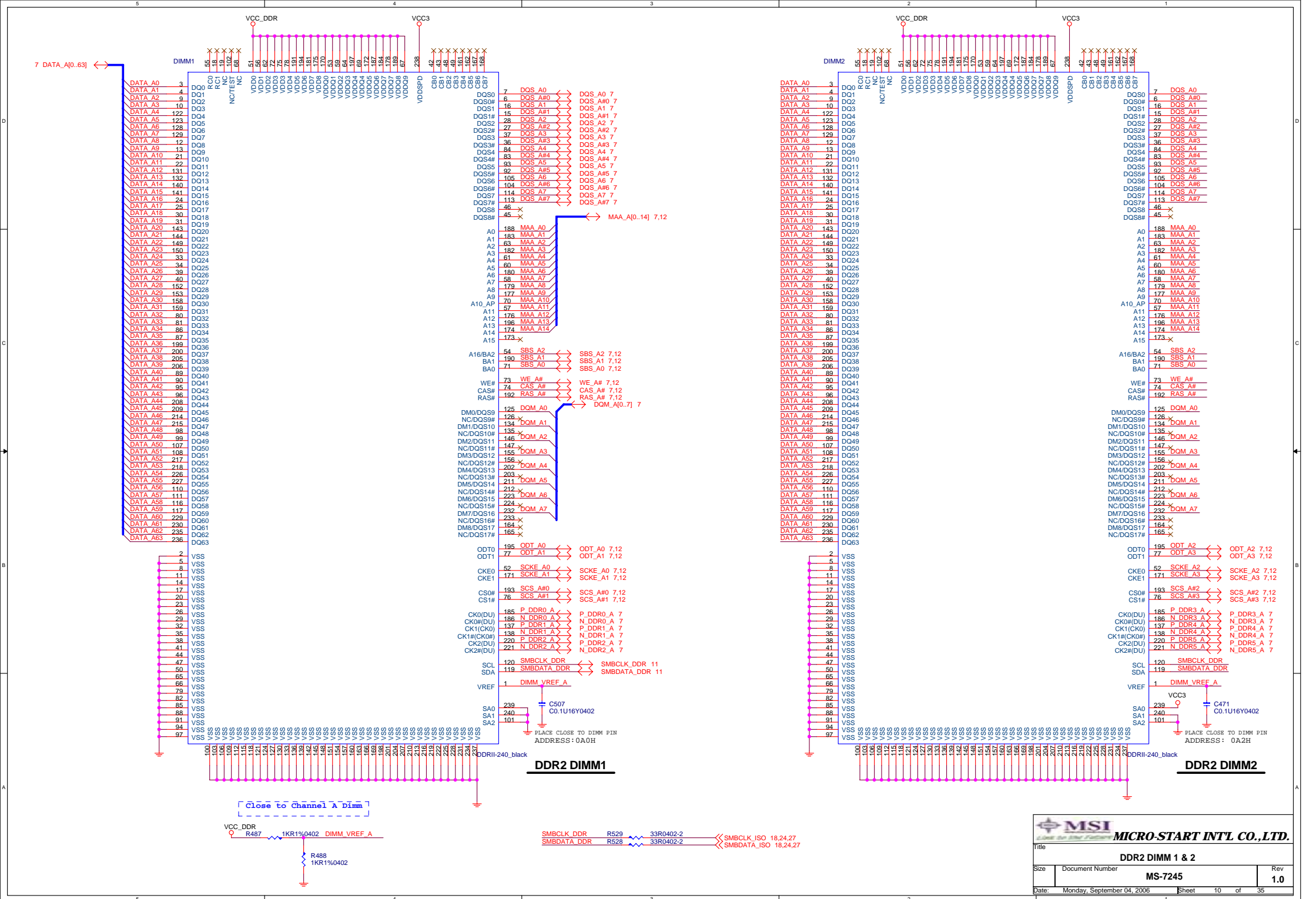
Place these caps within socket cavity

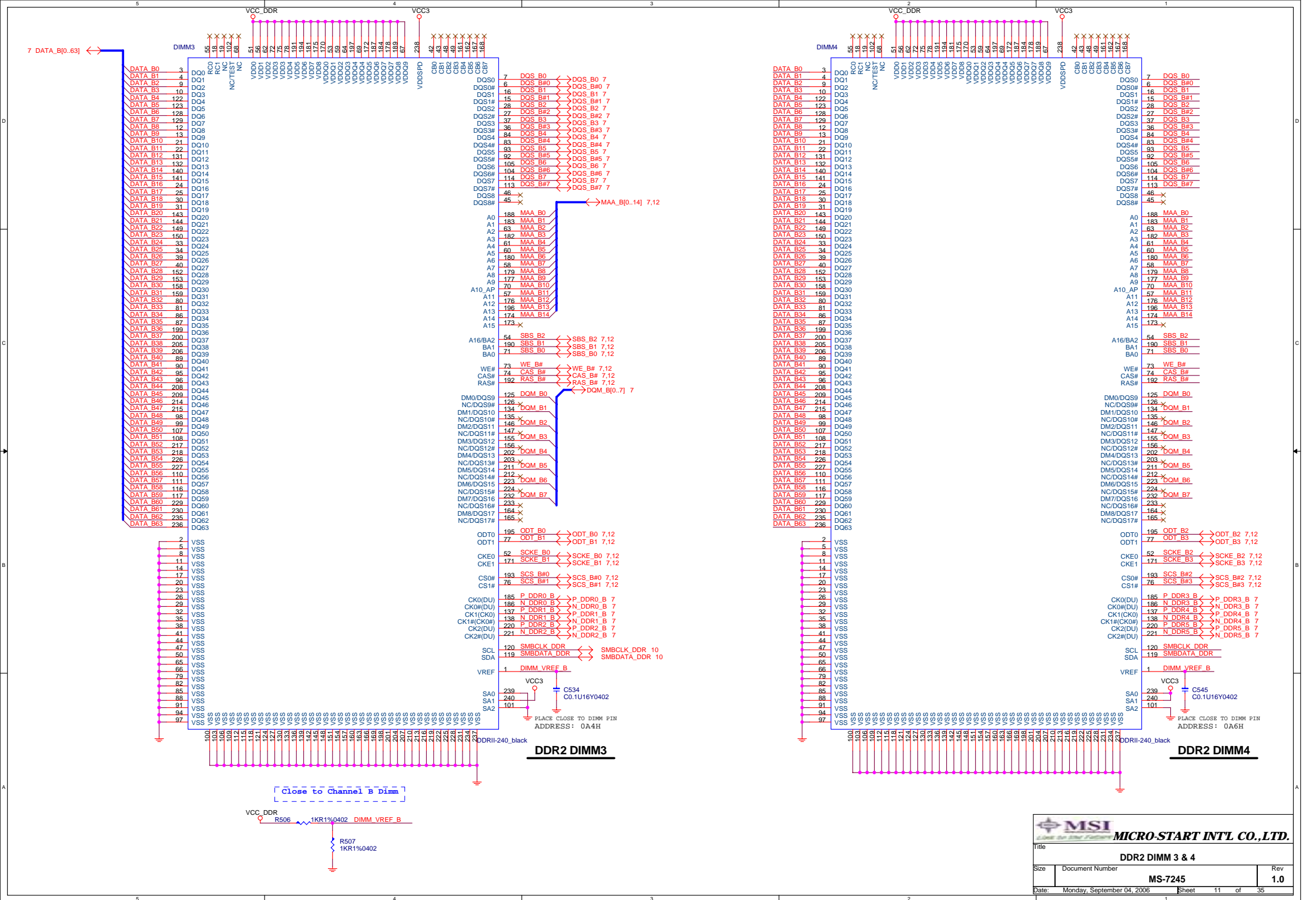




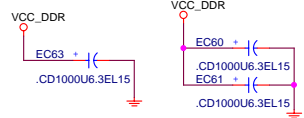
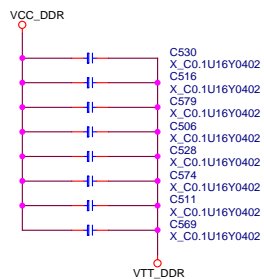
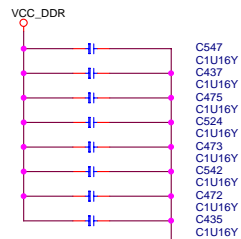
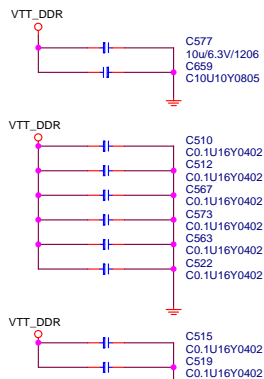
V_1P25_CORE



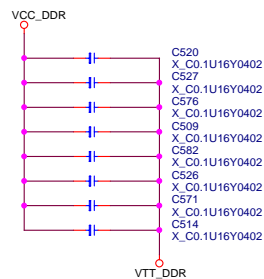
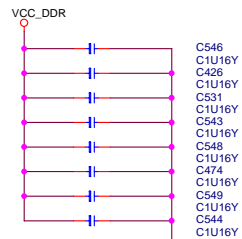
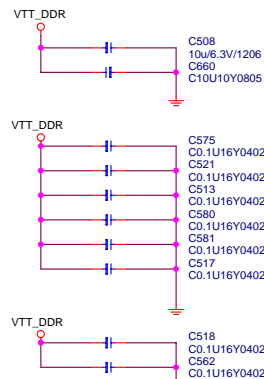




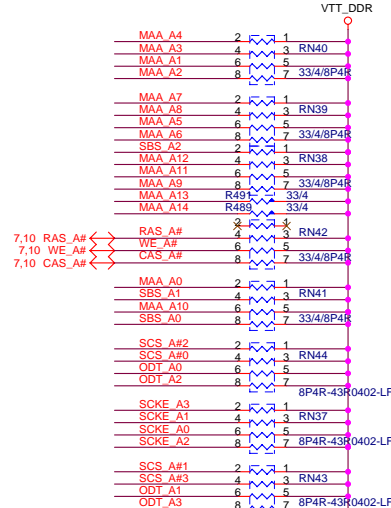
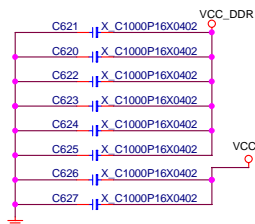
CHANNEL A V_SM_VTT DECOUPLING CAPS



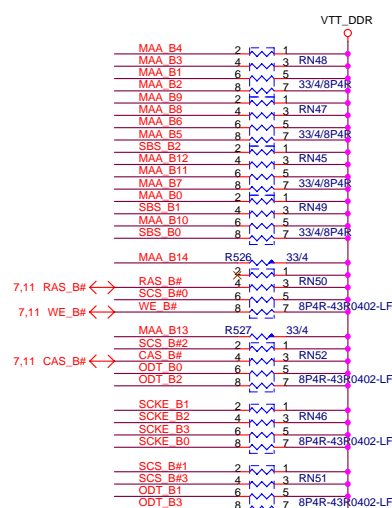
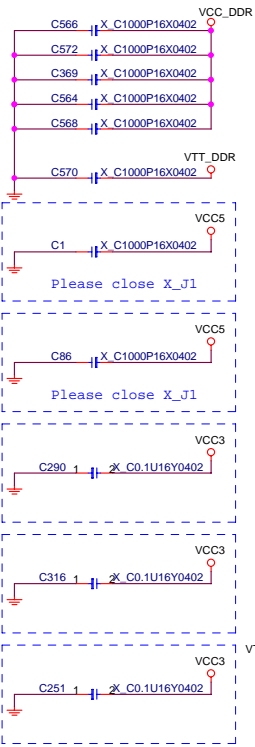
CHANNEL B V_SM_VTT DECOUPLING CAPS



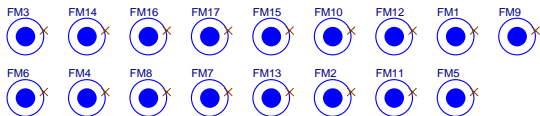
EMI CAPS reserve



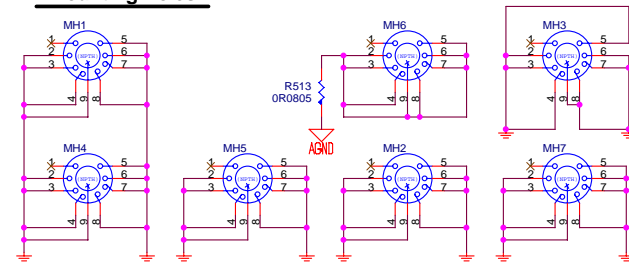
EMI CAPS reserve



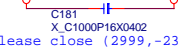
Optical Fiducial Marks



Mounting Holes

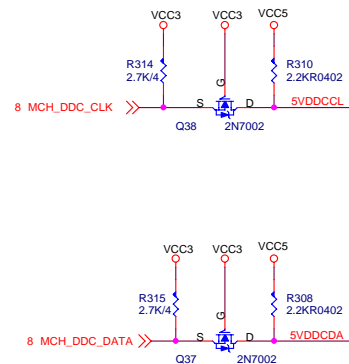
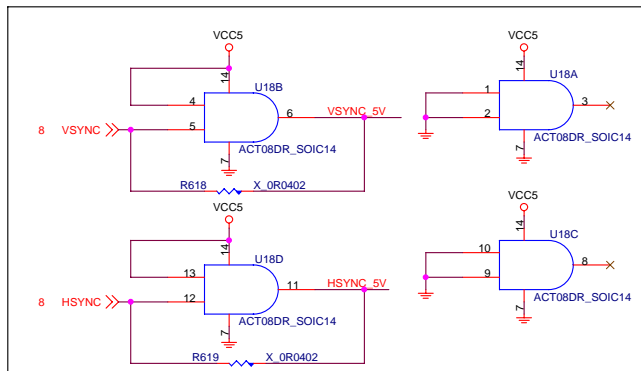
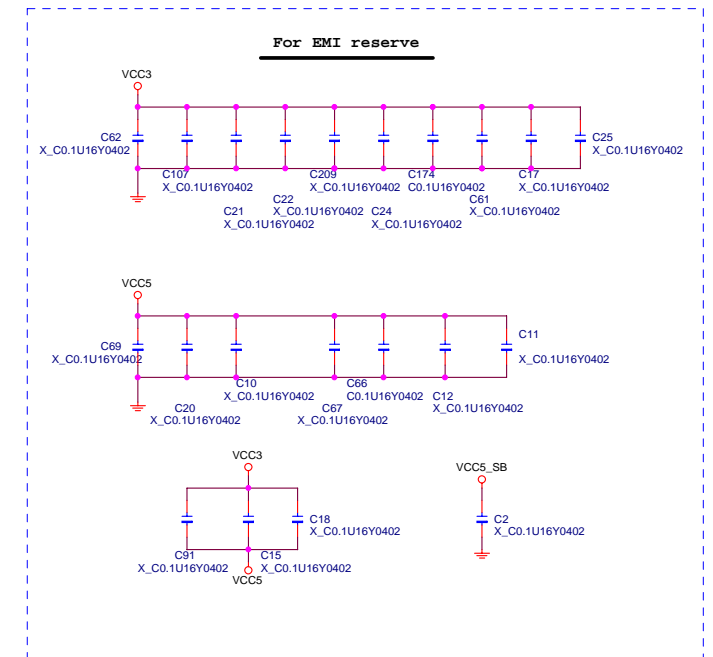
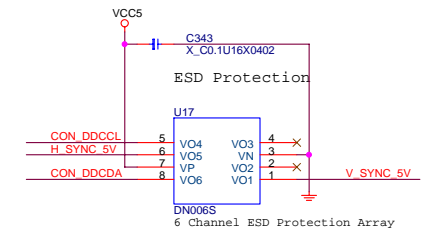
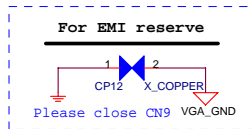
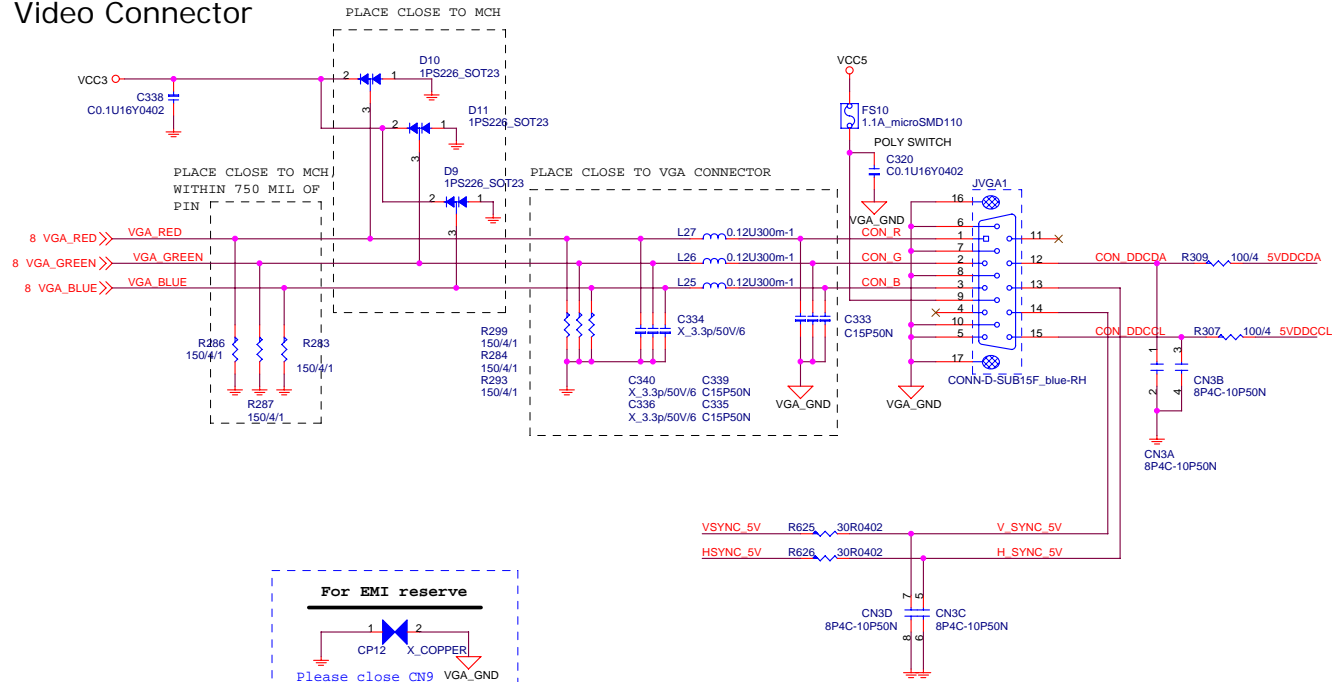


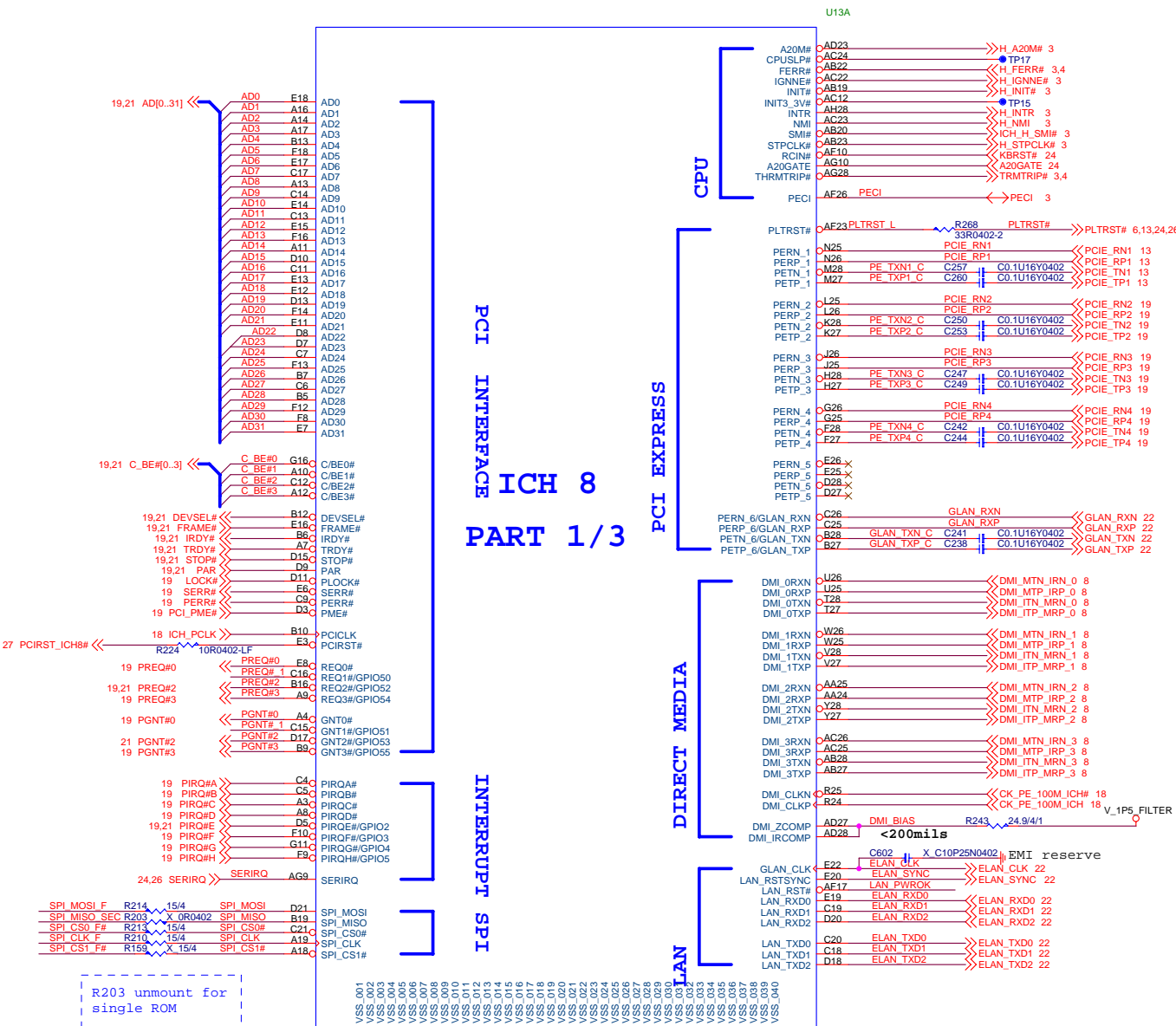
For EMI reserve



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Video Connector



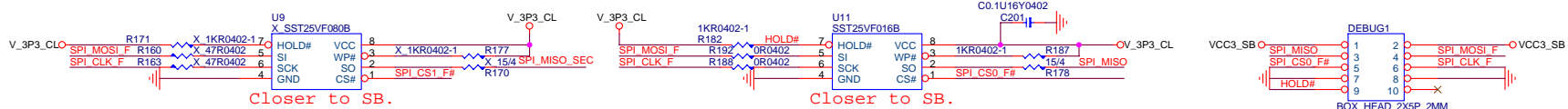


ICH 8
PART 1/3

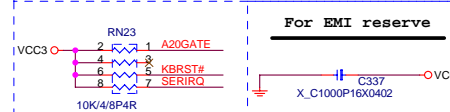
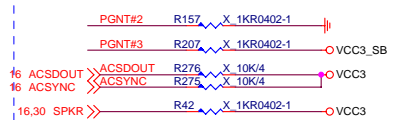
SPI FLASH(8M) (16M)

Note:MT3H stuff 8M

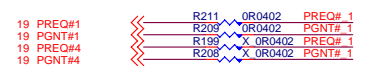
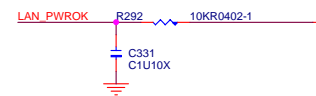
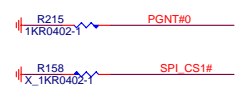
SPI Debug Port




ICH8 H/W STRAPS			
SIGNAL	H	L	DES.
SPKR	DIS	EN	REBOOT
GNT3	DIS	EN	A16 OVERRIDE
INTVRMEN	EN	DIS	INT VRM
SATALED	NORM	REVERSE	PCIE 0-3 ORDER
HDA_SDOUT	DFX/PCIE	N/A	XOR MODE/PCIE PORT CONFIG
HDA_SYNC	SET BIT	N/A	PCIEPORT CONFIG BIT 0 (1-4)
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)



BOOT SELECT STRAPS			
BOOT DEVICE	GNT0	SPI_CS1#	
FWH	1	1	
SPI	0	X	(Default)
PCI	1	0	

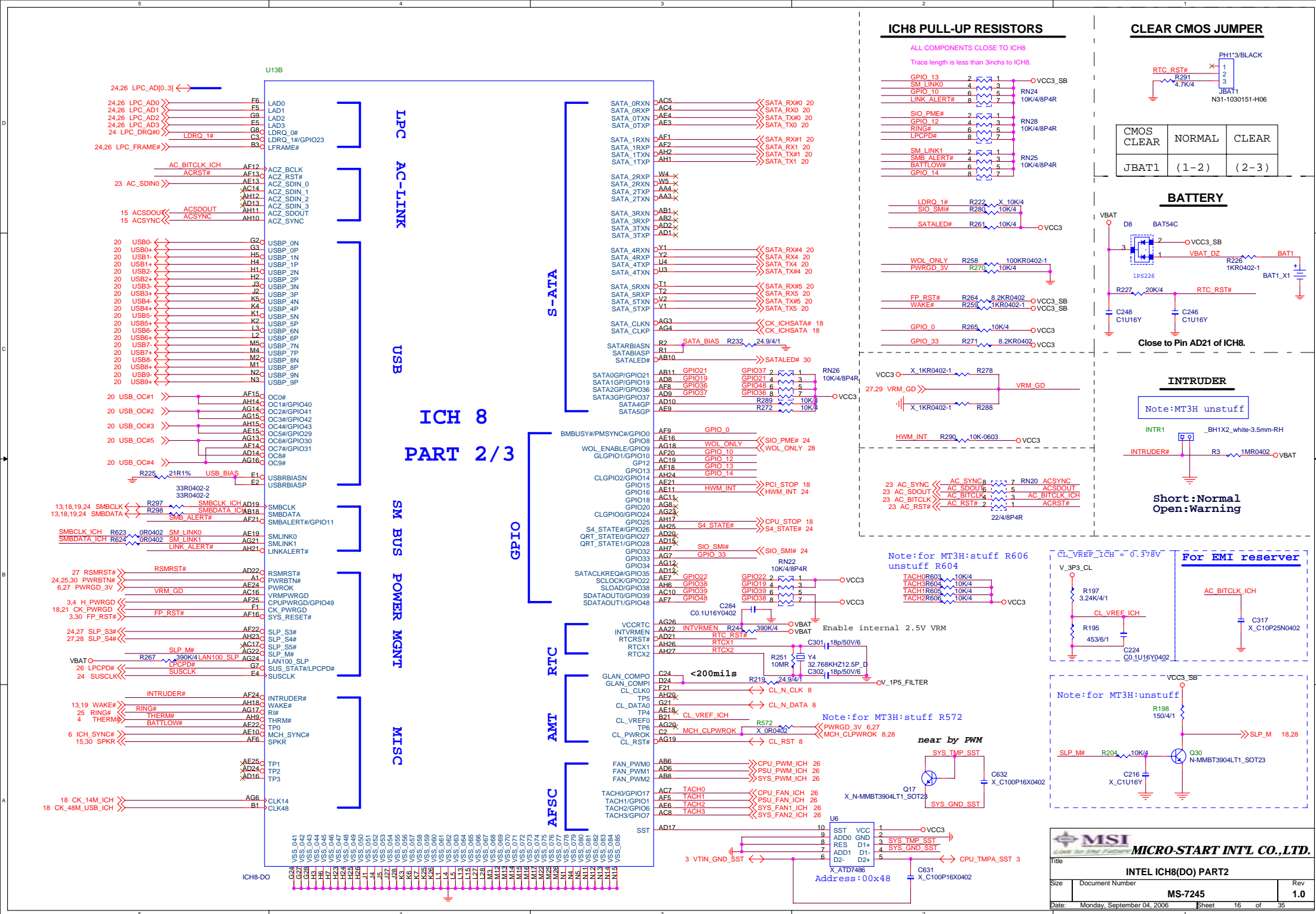


STD:R211,R209 Mount,R199,R208 unmount
For NEC daughter card: R199,R208 Mount
R211,R209 Remove

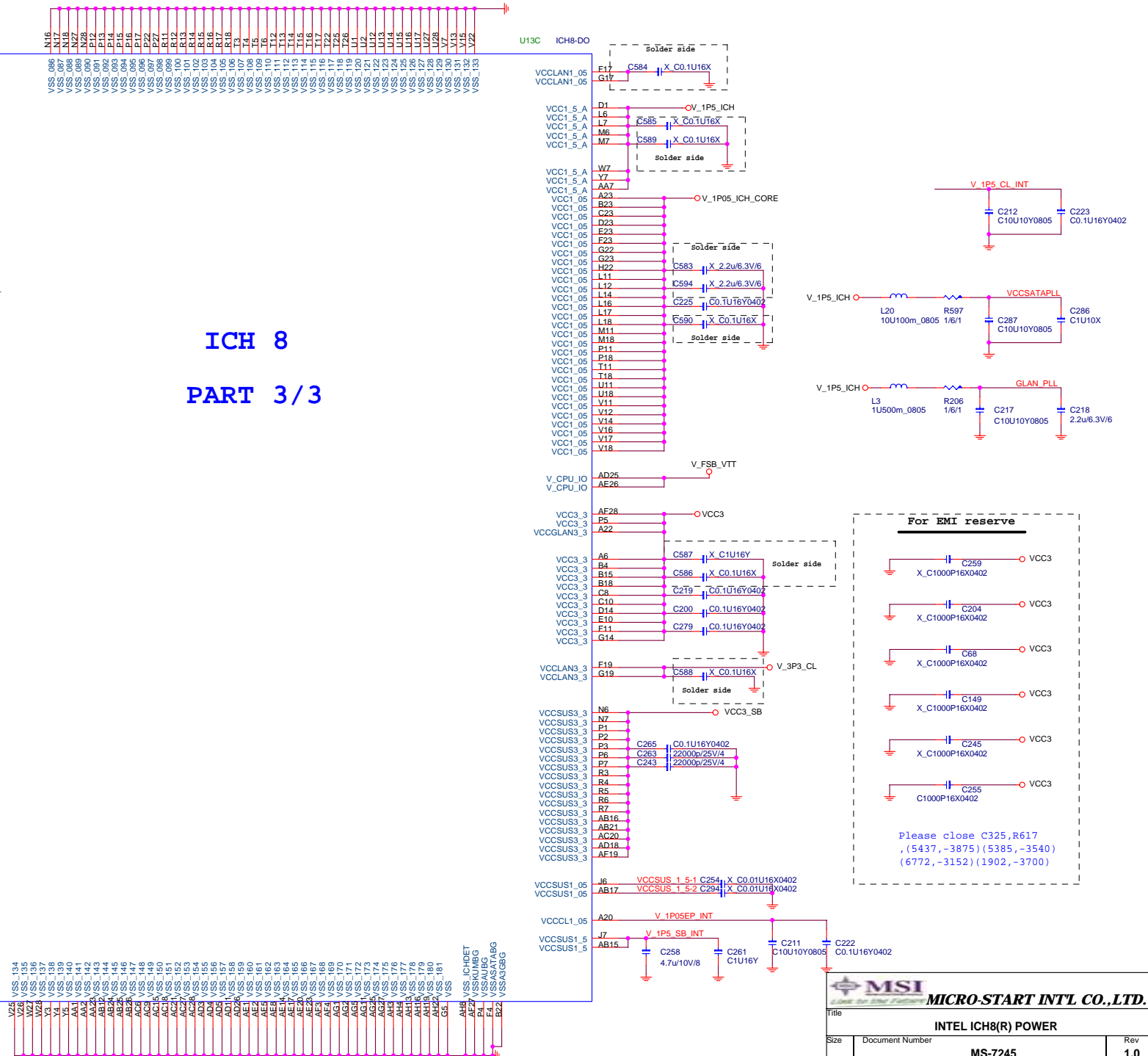


MICRO-START INTL CO.,LTD.

Title		
INTEL ICH8(R) PART1		
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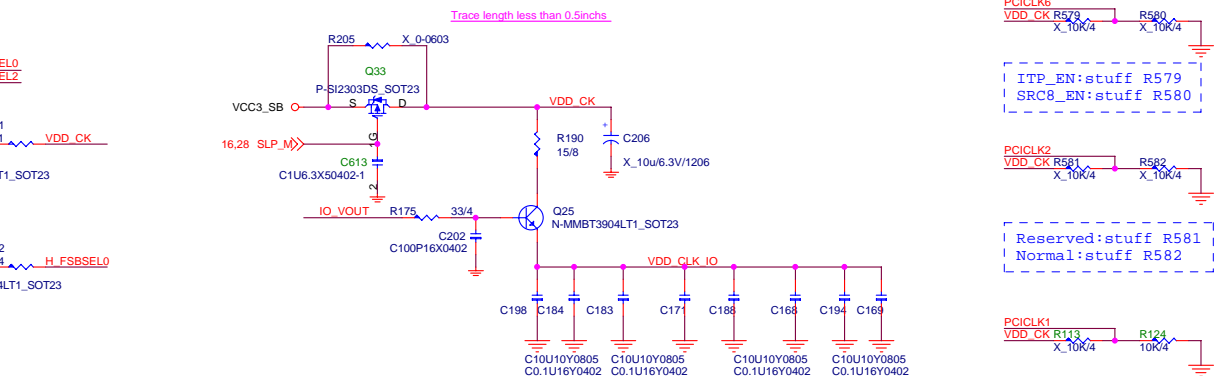
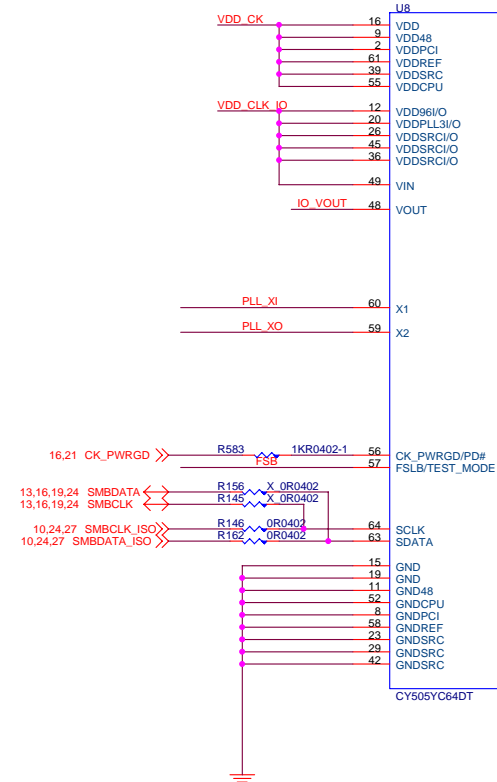
ICH 8
PART 3/3



```

Please put all caps close CLK GEN.

```



Note:for MT3H
 Stuff:R113
 Untuff:R124

PCICLK6

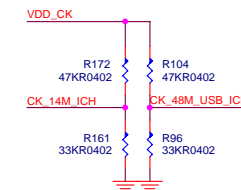
VDD CK R579 R580

X_10K/4 X_10K/4

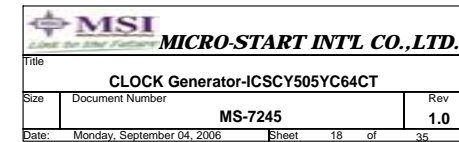
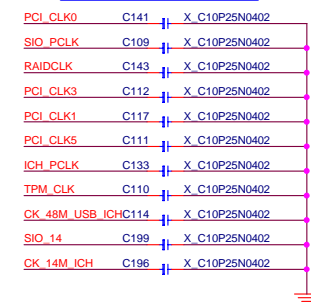
ITP_EN:stuff R579

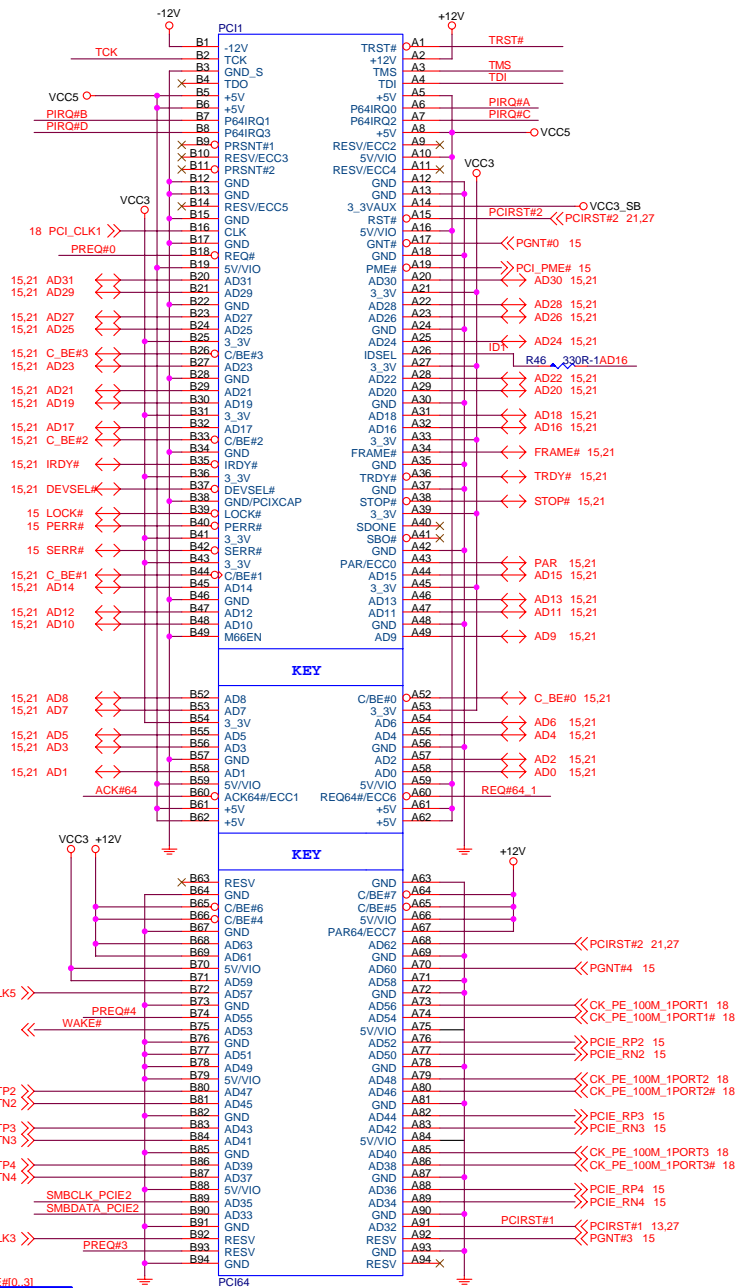
SRC8_EN:stuff R580

3,4,8	H_FSBSEL1	H_FSBSEL1	R155	1KR0402-1	FSB
3,4,8	H_FSBSEL0	H_FSBSEL0	R95	X_10K/4	USB 48M
3,4,8	H_FSBSEL2	H_FSBSEL2	R181	X_10K/4	CK 14M



For EMI reserver



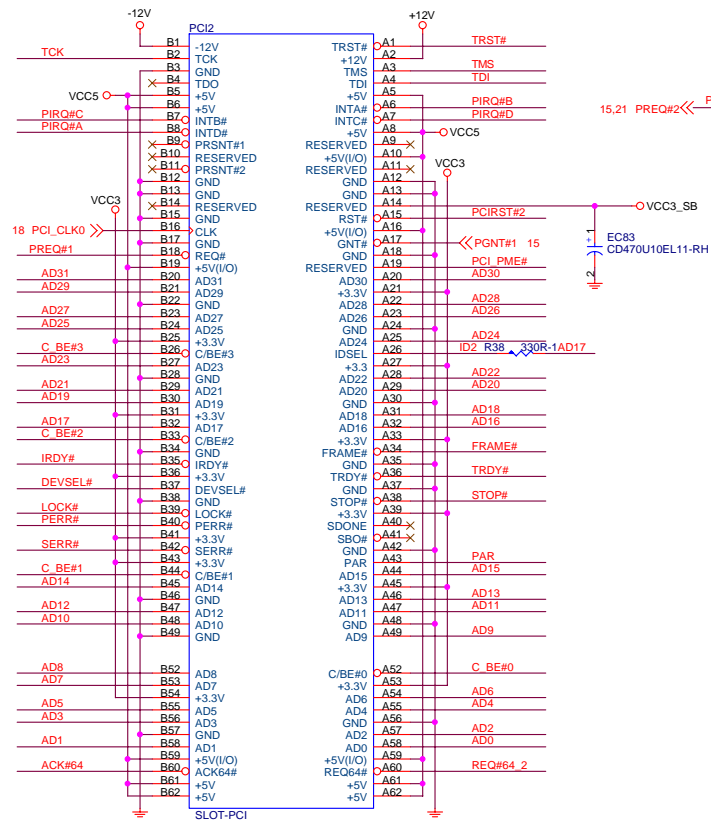
PCI1/PCIEXTENT

```

IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

```

```
PCI3 RESERVE
IDSEL = AD18
MASTER = PREQ#3
PIRQ#C
```

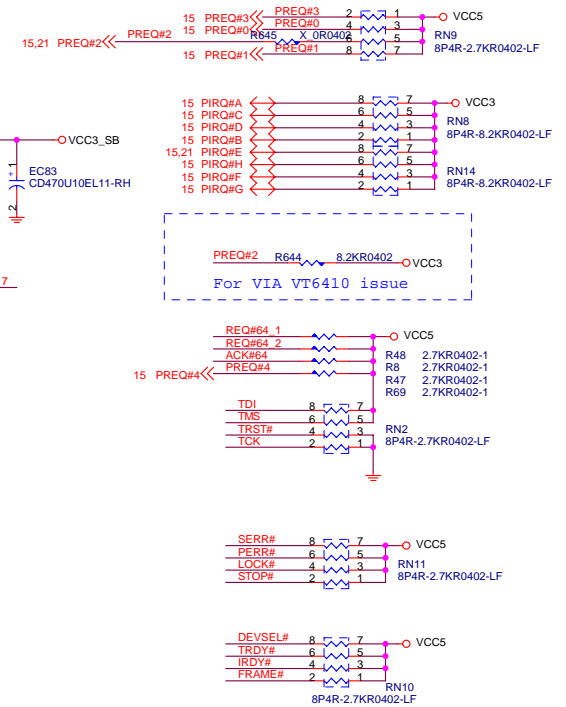
PCI SLOT 1 (PCI VER: 2.3 COMPLY)

IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

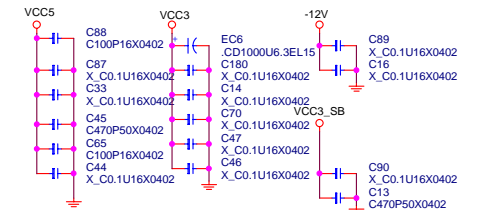
For EMI reserve

+12V
C84 X C0.01U16X0402

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

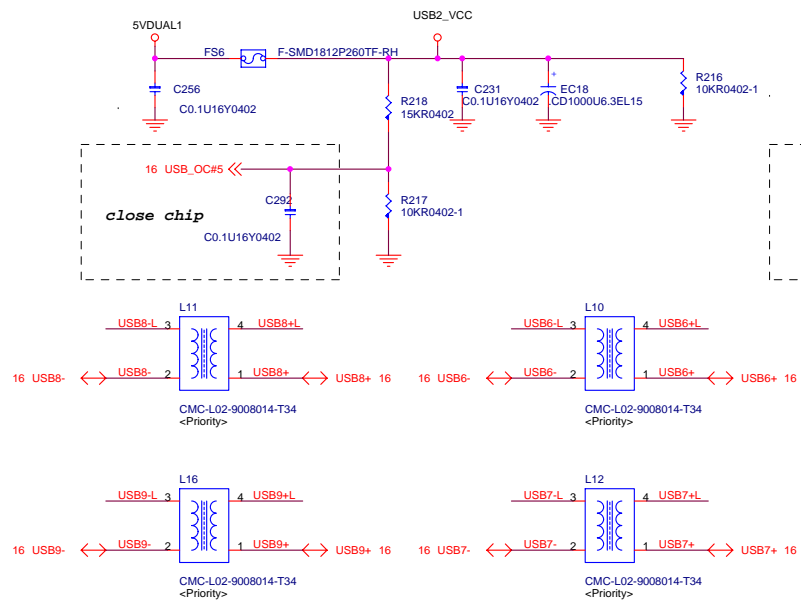


MICRO-START INT'L CO., LTD.

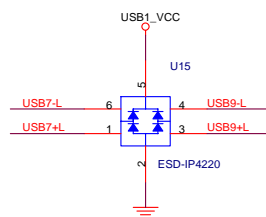
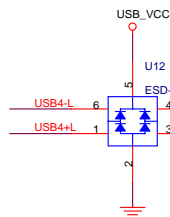
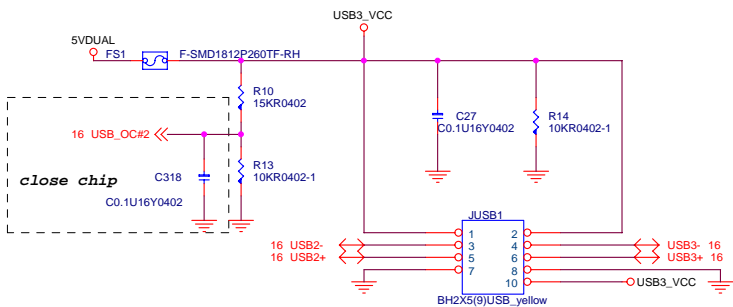
Title	PCI1EXTENDER/PCI2
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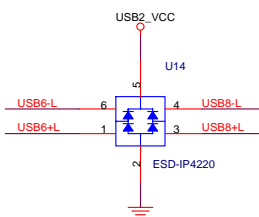
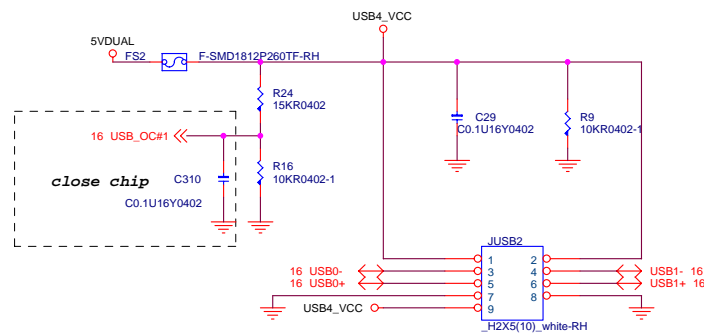
POWER CIRCUIT FOR USB PORT 6,7,8,9 (REAR)



EXTERNAL USB PORT 2,3

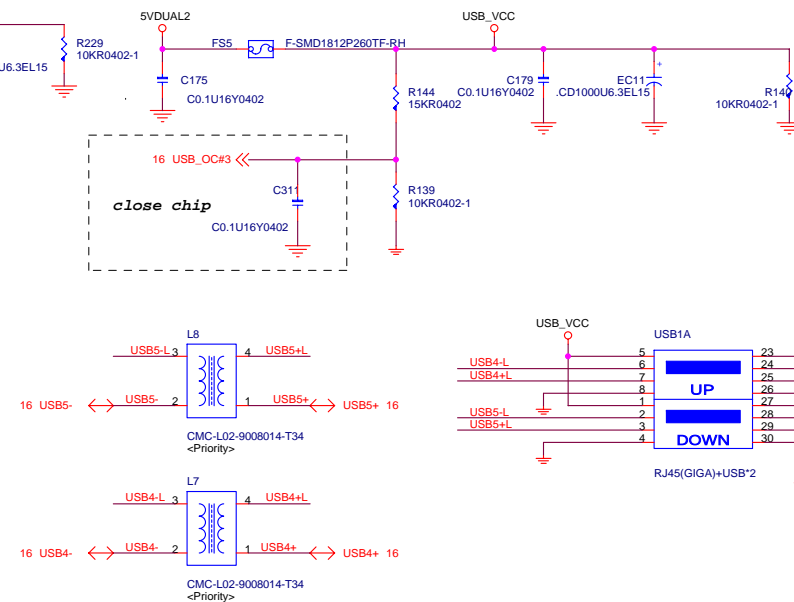


EXTERNAL USB PORT 0,1

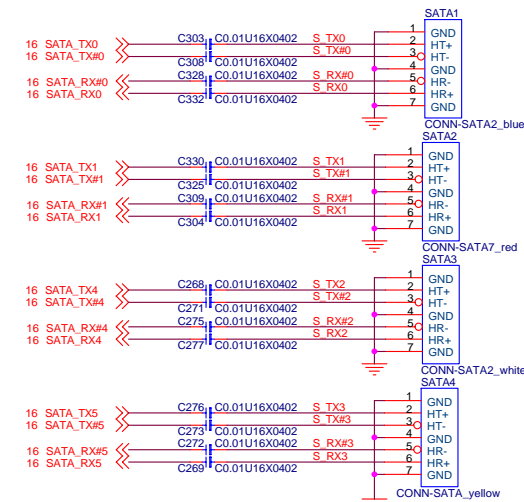


For EMI reserve
VCC5
C341
C1000P16X0402
Please close SATA2 connector

EXTERNAL USB PORT 4,5(REAR)

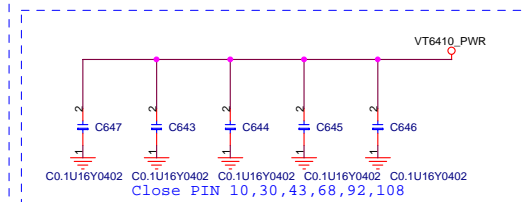
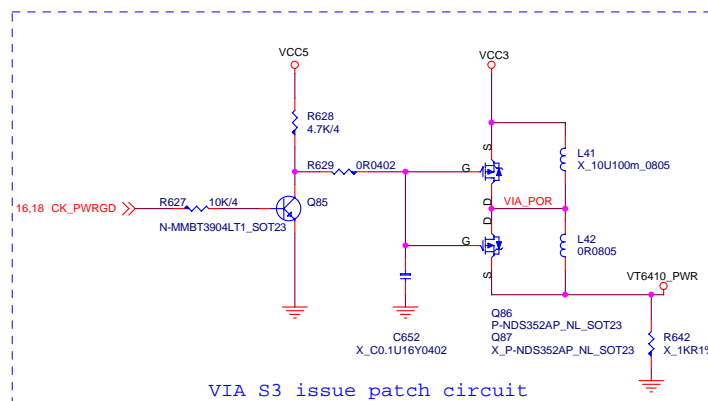
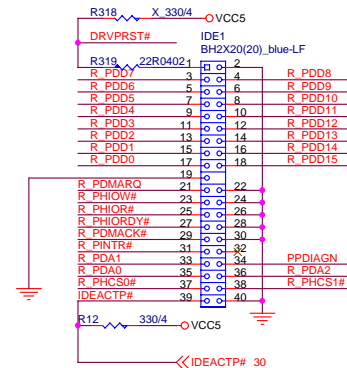
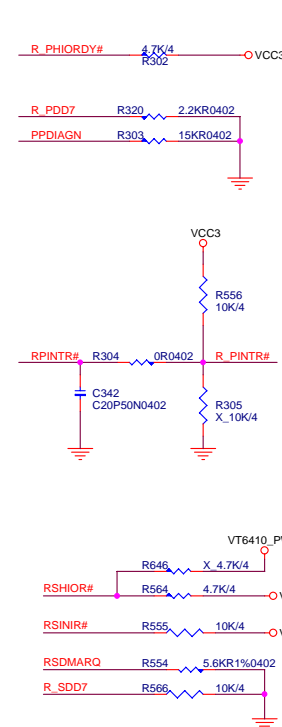
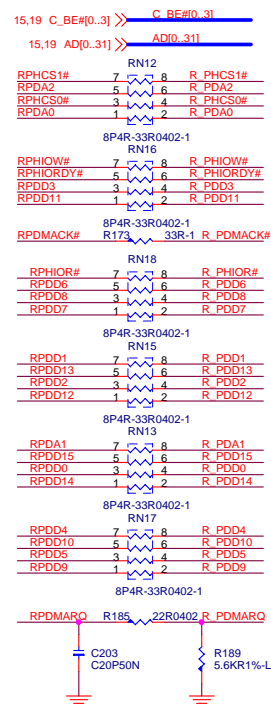
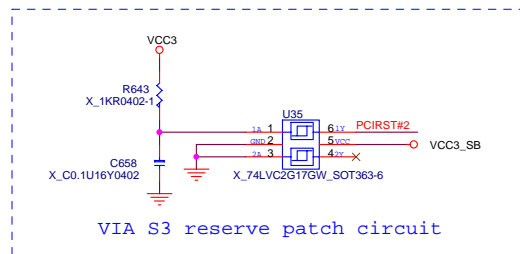


SERIAL ATA CONNECTOR BLOCK

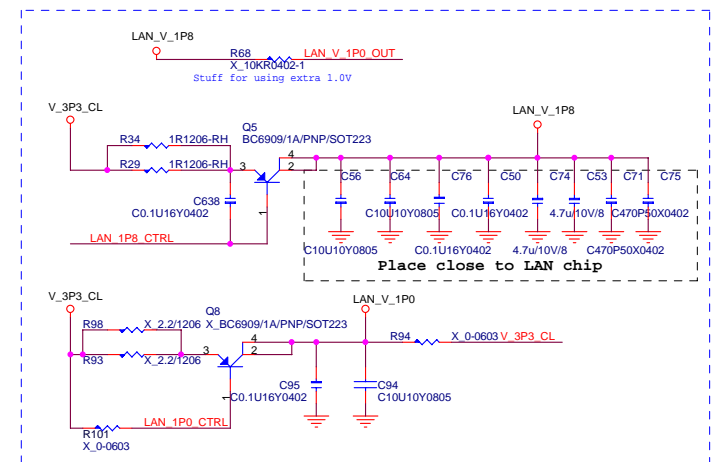
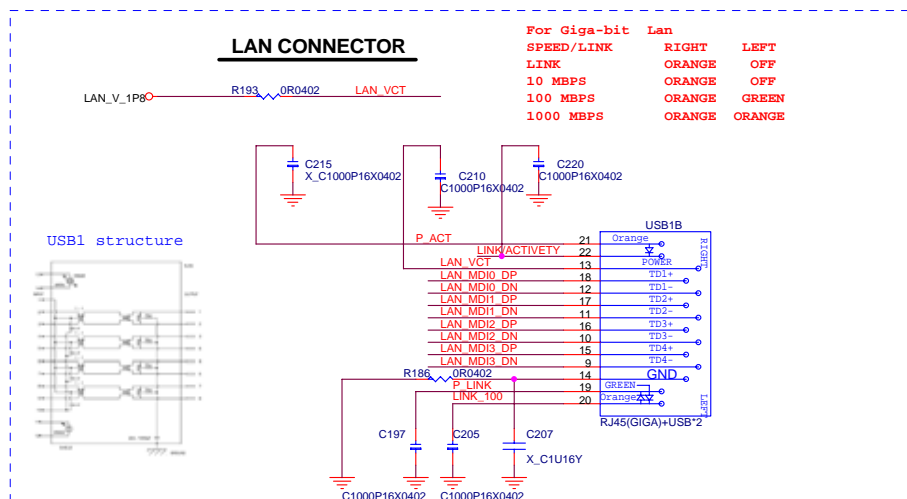
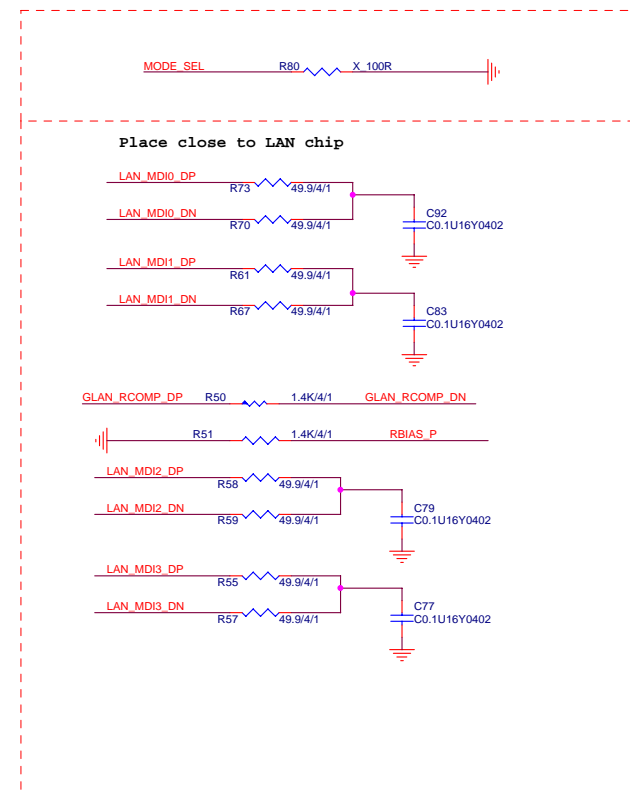
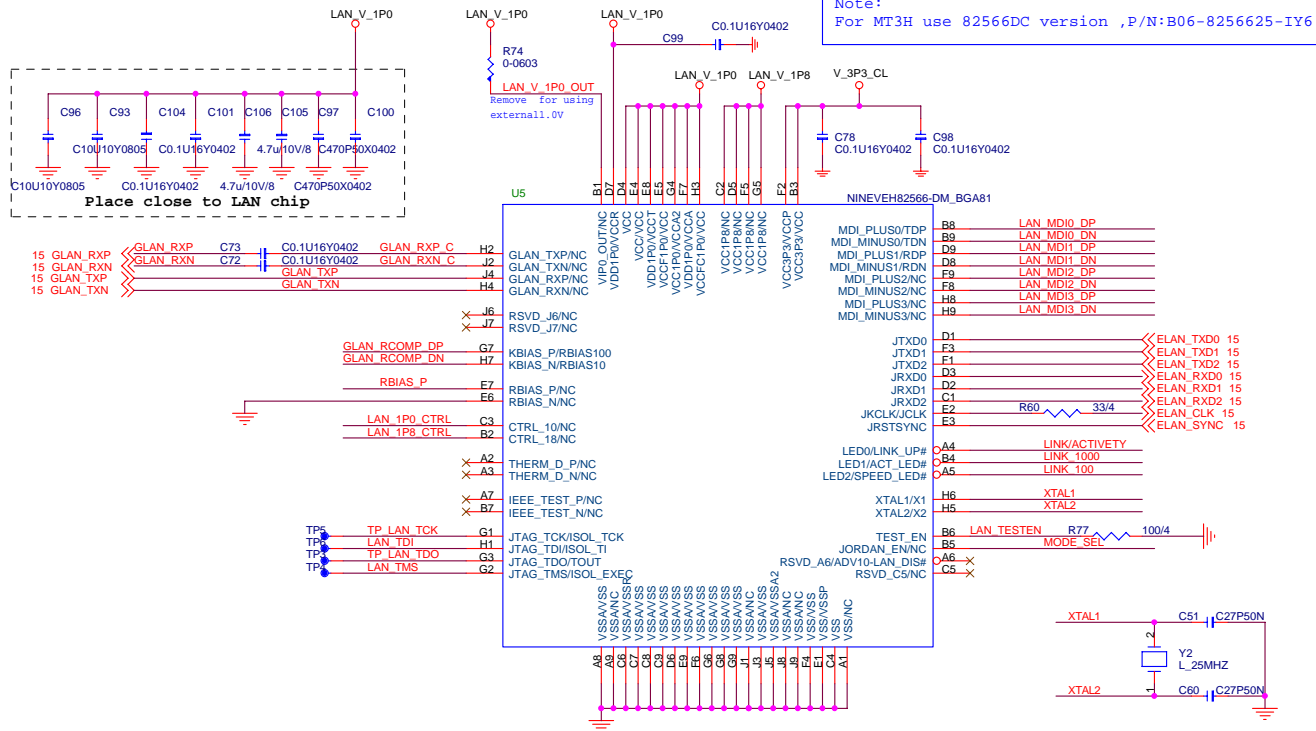


SATA USB		
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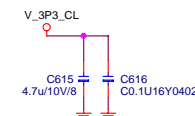
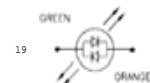
```
IDSEL = AD20
MASTER = PREQ#2
PIRQ#E
```



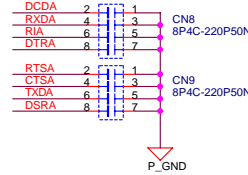
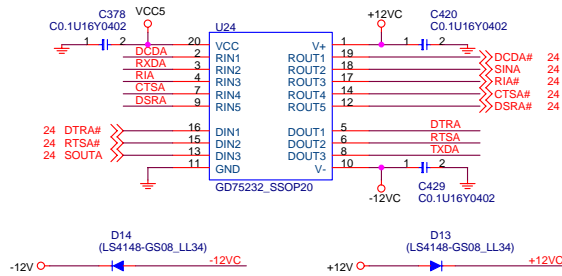
LAN - NINEVEH



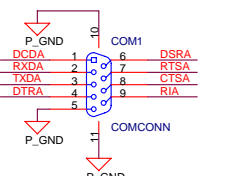
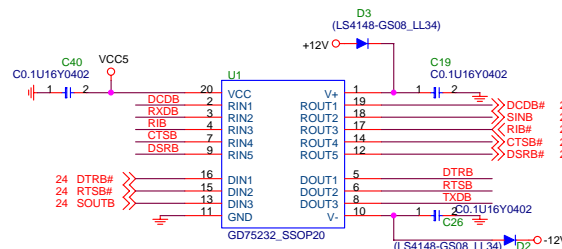
ACT_LED	Link_LED
S0: LOW	S0: LOW
S1/S3/S4/S5: HIGH	S5: HIGH
	S1/S3/S4: WOL EN-->LOW WOL DIS-->HIGH



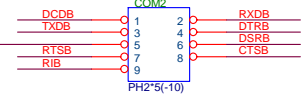
SERIAL PORT 1



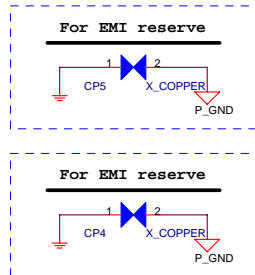
SERIAL PORT 2



COM2 HEADER

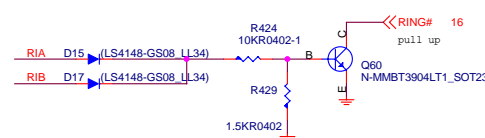


K/B Power supply function for NEC



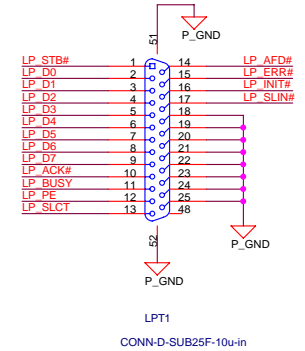
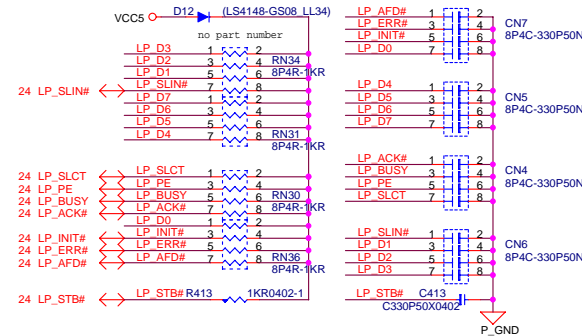
GPIO_KB
HI:VCC5_KB = USB1_VCC
LOW:VCC5_KB = VCC5_SB
VCC_DUAL(USB1_VCC)
S0/S1:VCC5
S3:VCC5_SB
S4/S5:0V

Wake On Modem Header

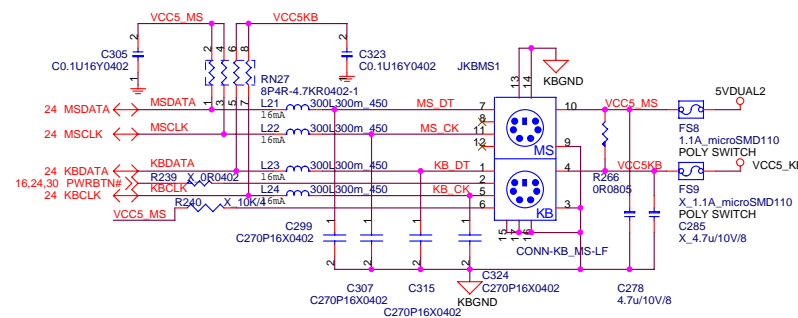


PARALLAL PORT

24 LP_D[0..7] ↔ LP_D[0..7]



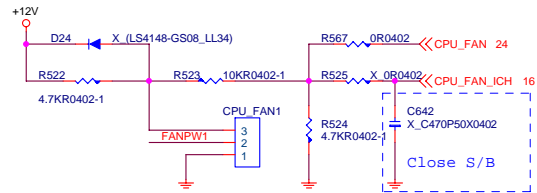
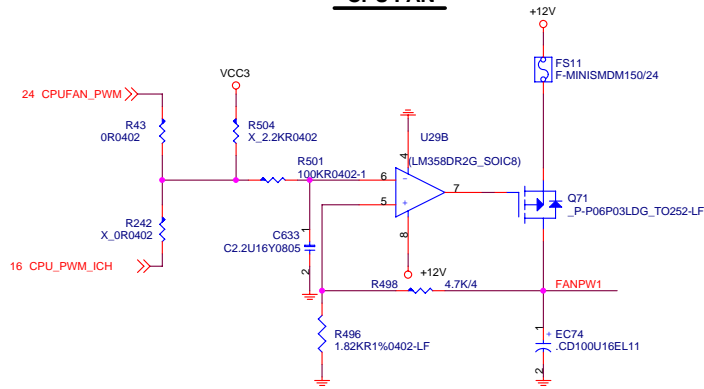
PS2 KEYBOARD & MOUSE CONNECTOR



MSI MICRO-START INTL CO.,LTD.

Title KB/MS LPT COM FAN
Size Document Number MS-7245 Rev 1.0
Date: Monday, September 04, 2006 Sheet 25 of 35

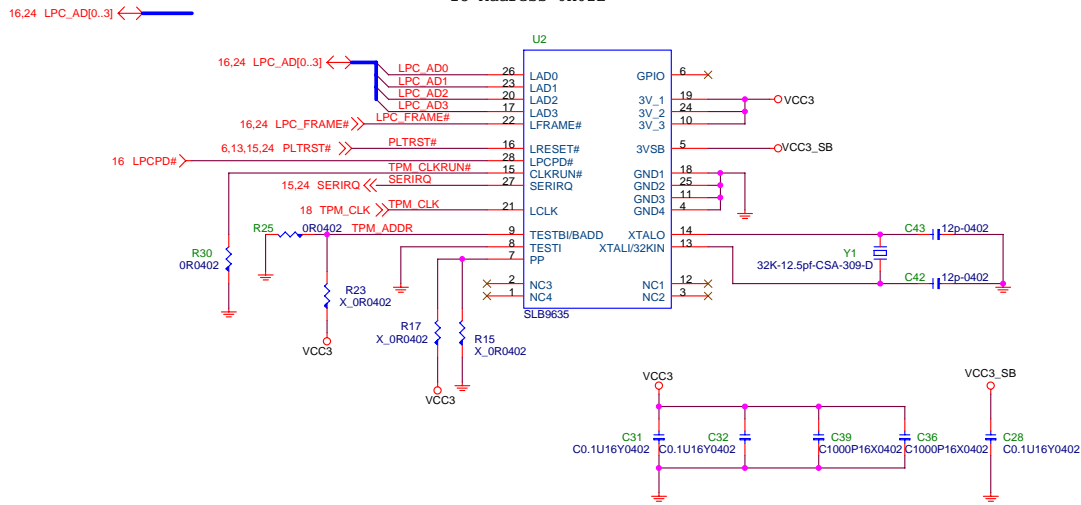
CPU FAN



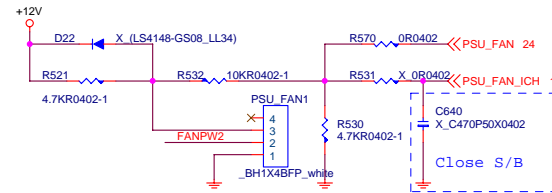
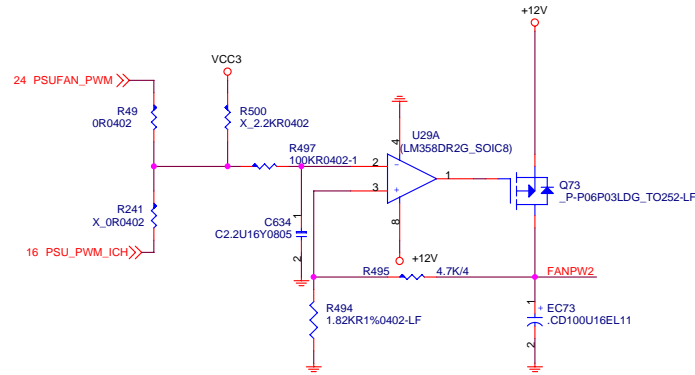
TPM 1.2

Note:MT3H unstuff (plesae see page35)

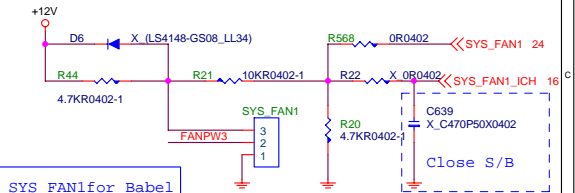
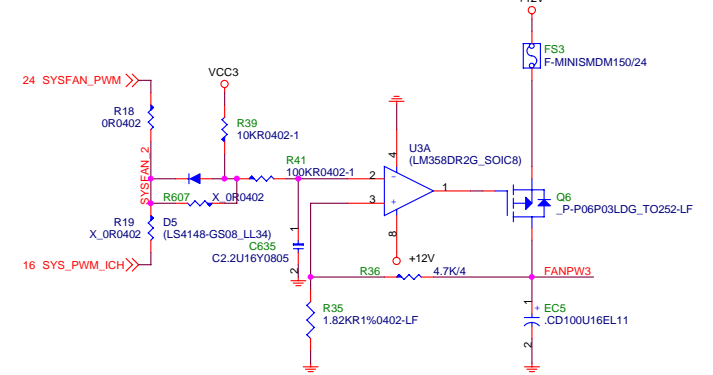
IO Address:0x02E



PSU FAN

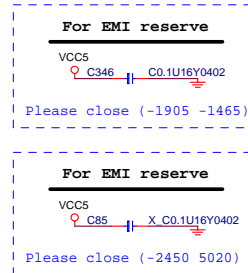
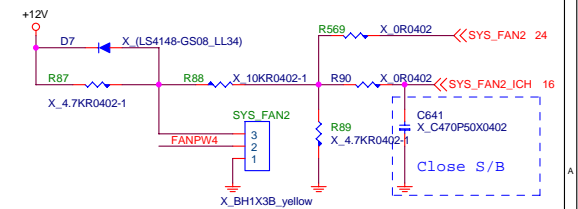
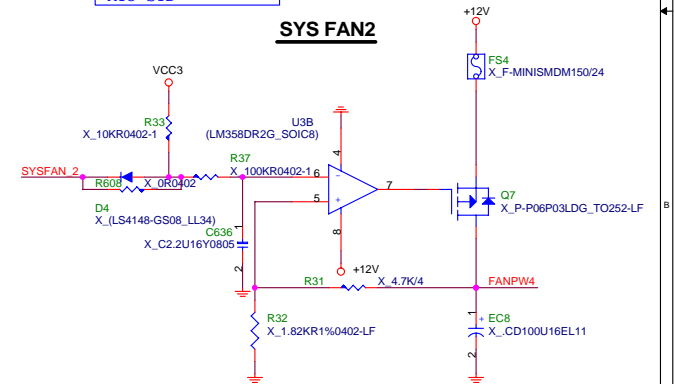


SYS FAN1



SYS_FAN1for Babel
Babel:right angle
SYS_FAN2 for MT3H
MT3:STD

SYS FAN2



SOT23

Page 106

VCC5 SB 9VSB

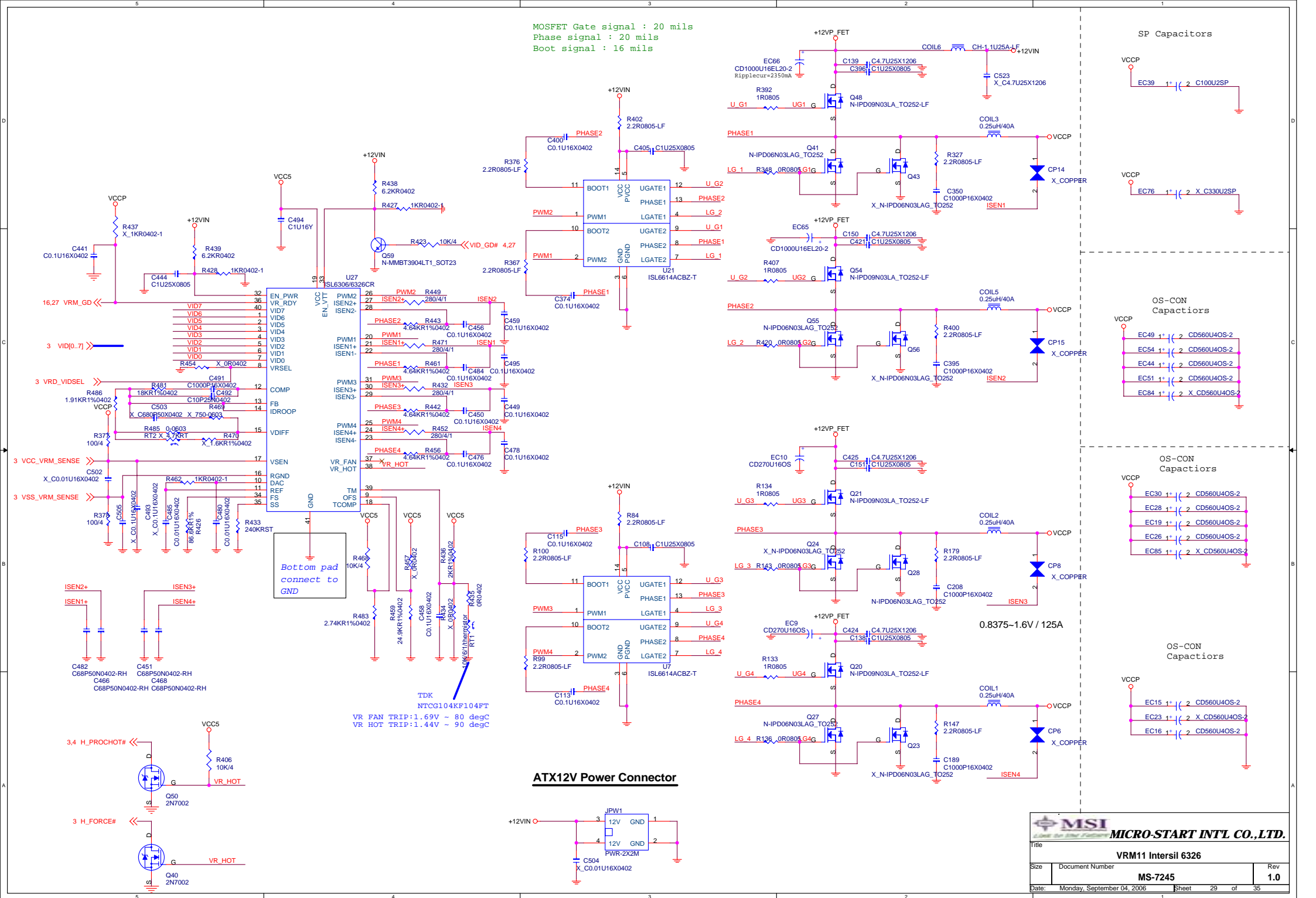


(111111)

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MOSFET Gate signal : 20 mils
Phase signal : 20 mils
Boot signal : 16 mils



Front Panel

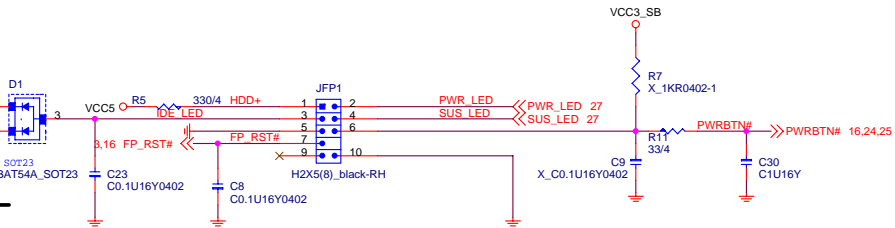
IDE LED

21 IDEACTP# >>
Active-low

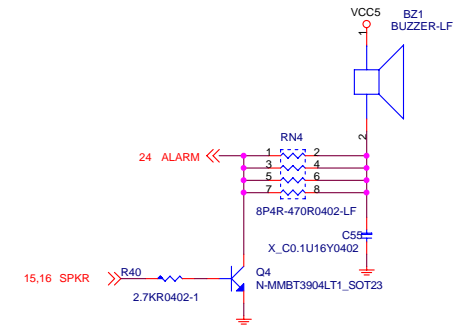
Active-low

SERIAL ATA LED

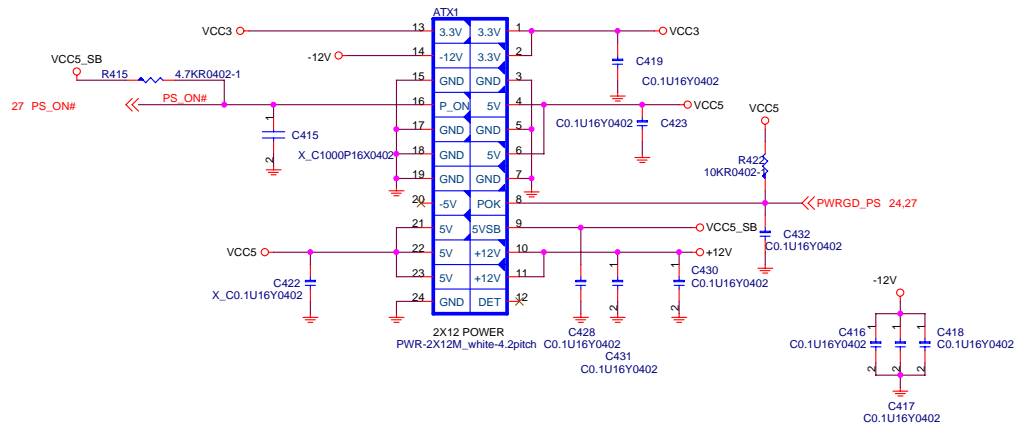
16 SATALED# >>



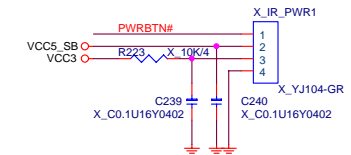
SPEAKER



ATX Connector



For NEC IR POWER



ICH8

GPIO Pin	Type	Default	Function	Power	MUXED/ UNMUXED	Pin-out
GPIO 0	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF9
GPIO 1	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AF5
GPIO 2	I/O	GPI	PIRQ#E pull-up to VCC3 with 10K	VCC3		D5
GPIO 3	I/O	GPI	PIRQ#F pull-up to VCC3 with 10K	VCC3		F10
GPIO 4	I/O	GPI	PIRQ#G pull-up to VCC3 with 10K	VCC3		G11
GPIO 5	I/O	GPI	PIRQ#H pull-up to VCC3 with 10K	VCC3		F9
GPIO 6	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE6
GPIO 7	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AC8
GPIO 8	I/O	GPI	SIO_PME# connect to SIO,pull_up VCC3_SB with 10k	VCC3_SB	UNMUXED	AE16
GPIO 9	I/O	MGPIO3	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AG18
GPIO 10	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AF20
GPIO 11	I/O	SMBALERT#	SMB_ALERT# pull-up to VCC3_SB with 10K	VCC3_SB		AF21
GPIO 12	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VBT	UNMUXED	AC19
GPIO 13	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	UNMUXED	AF18
GPIO 14	I/O	GPI	Pull-up to VCC3_SB with 10K directly	VCC3_SB	MUXED	AH24
GPIO 15	I/O	GPO	PCI_STOP	VCC3_SB	UNMUXED	AE21
GPIO 16	I/O	GPO	SIO HWM_INT,pull_up VCC3 with 10K(change to GPI)		UNMUXED	AE11
GPIO 17	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AC7
GPIO 18	I/O	GPO	NC		UNMUXED	AC11
GPIO 19	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AD8
GPIO 20	I/O	GPO	NC		UNMUXED	AG8
GPIO 21	I/O	GPI	Pull-up to VCC3 with 10K	VCC3		AB11
GPIO 22	I/O	GPI	Pull-up to VCC3 with 10K	VCC3	MUXED	AE7
GPIO 23	I/O	LDRQ1#	LDRQ_1# pull_up VCC3 with 10K	VCC3	MUXED	C3
GPIO 24	I/O	GPO	NC		MUXED	AG23
GPIO 25	I/O	GPO	CPU_STOP	3.3V_SB	UNMUXED	AH17
GPIO 26	I/O	GPO	S4 STATE			AH25
GPIO 27	I/O	GPO	NC	3.3V_SB		AD20
GPIO 28	I/O	GPO	NC			AD15
GPIO 29	I/O	OC5#	OC#3 connect to USB connector	3.3V_SB		AE15
GPIO 30	I/O	OC6#	OC#4 connect to USB connector	3.3V_SB		AG13
GPIO 31	I/O	OC7#	OC#4 connect to USB connector	3.3V_SB		AF14
GPIO 32	I/O	GPO	SIO_SMI# connect to SIO,pull up VCC3 with 10k	VCC3	UNMUXED	AH7
GPIO 33	I/O	GPO	Pull-up to VCC3 with 8.2K		UNMUXED	AG7
GPIO 34	I/O	GPO	NC		UNMUXED	AG12
GPIO 35	I/O	GPO	NC			AD12
GPIO 36	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF8
GPIO 37	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AD9
GPIO 38	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AH6
GPIO 39	I/O	GPI	Pull-down to GND with 10K directly	VCC3		AC10
GPIO 40	I/O	OC1#	OC#1 connect to USB connector	VCC3		AH14
GPIO 41	I/O	OC2#	OC#2 connect to USB connector	VCC3		AG14
GPIO 42	I/O	OC3#	OC#2 connect to USB connector	VCC3		AG15
GPIO 43	I/O	OC4#	OC#3 connect to USB connector	VCC3		AH15
GPIO 48	I/O	GPI	Pull-up to VCC3 with 10K directly	VCC3		AF7
GPIO 49	I/O	CPU_PWRGD	H_PWRGD connect to CPU	VTT_OUT		AF25
GPIO 50	I/O	REQ1#	REQ1 pull-up to VCC5 with 10K	VCC5	MUXED	C16
GPIO 51	I/O	GNT1#	GNT1#		MUXED	A15
GPIO 52	I/O	REQ2#	REQ2 pull-up to VCC5 with 10K	VCC5	MUXED	B16
GPIO 53	I/O	GNT2#	GNT2#		MUXED	D17
GPIO 54	I/O	REQ3#	REQ3 pull-up to VCC5 with 10K	VCC5	MUXED	A9
GPIO 55	I/O	GNT3#	GNT3#		MUXED	B9

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI1 EXTENT	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK1
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK0
VT6410	PIRQ#E	PREQ#2 PGNT#2	AD20	RAIDCLK
PCI3	RESERVED	PREQ#3 PGNT#3	AD18	PCI_CLK3

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	0A0H	SCLK_A0/SCLK_A0# SCLK_A1/SCLK_A1# SCLK_A2/SCLK_A2#
DIMM 2	0A2H	SCLK_A3/SCLK_A3# SCLK_A4/SCLK_A4# SCLK_A5/SCLK_A5#
DIMM 3	0A4H	SCLK_B0/SCLK_B0# SCLK_B2/SCLK_B2#
DIMM 4	0A6H	SCLK_B3/SCLK_B3# SCLK_B4/SCLK_B4# SCLK_B5/SCLK_B5#

SIO SCH5017


PIN NAME	PIN#	USAGE	Input/Output
GP43	92	GPIO_KB	OUTPUT
GP27	36	SIO_SMI#	OUTPUT
GP42	90	SIO_PME#	OUTPUT
INTRD_IN~	33	CLEAR_PASSWORD	INPUT

SMBus DISTRIBUTION

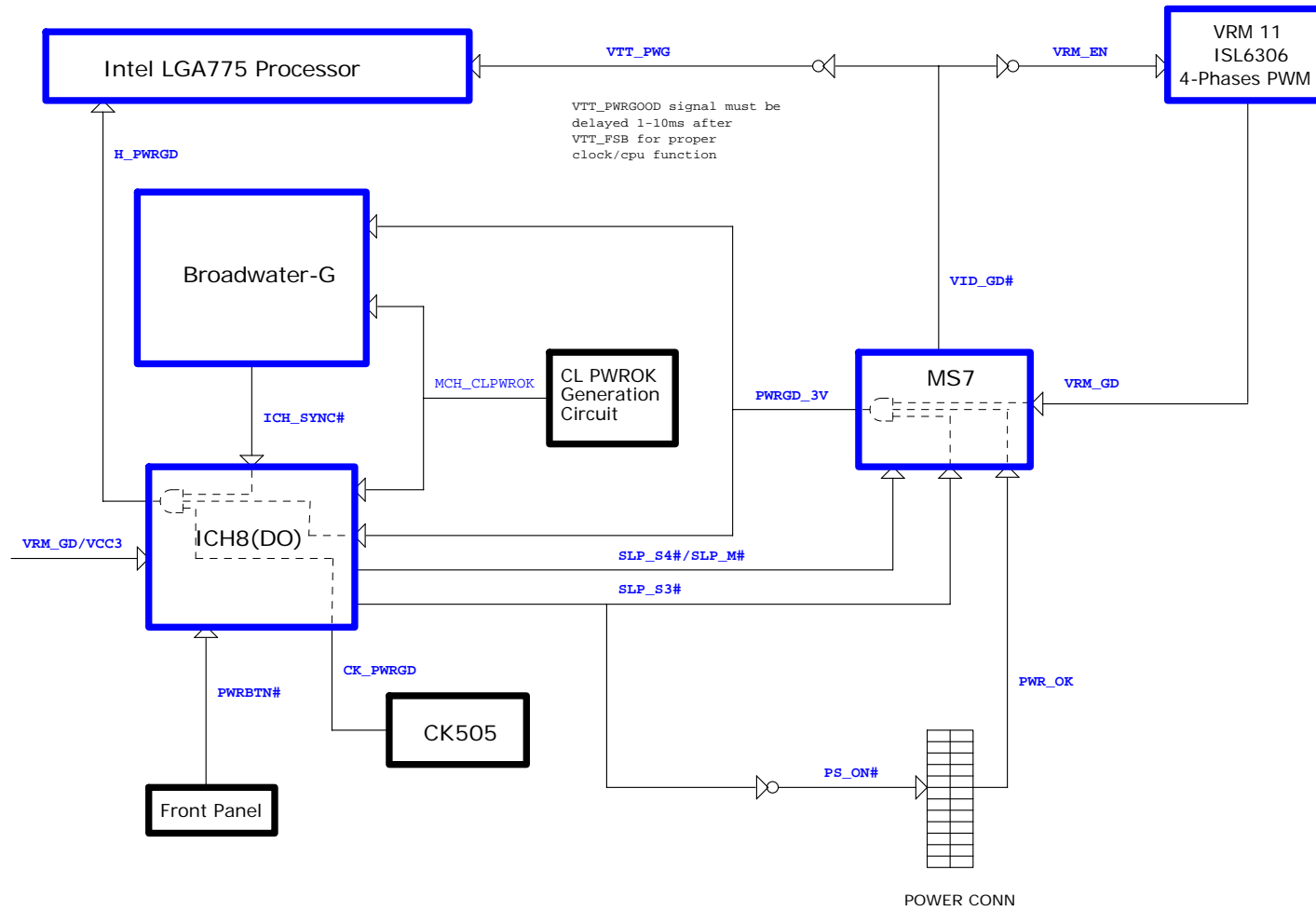
SMBus	Power	Load
SMBCLK	VCC3_SB	ICH8, SIO,PCI EXPRESS x16,x1
SMBCLK_ISO	VCC3	DIMM, CLK GEN, SIO, MS7,LAN

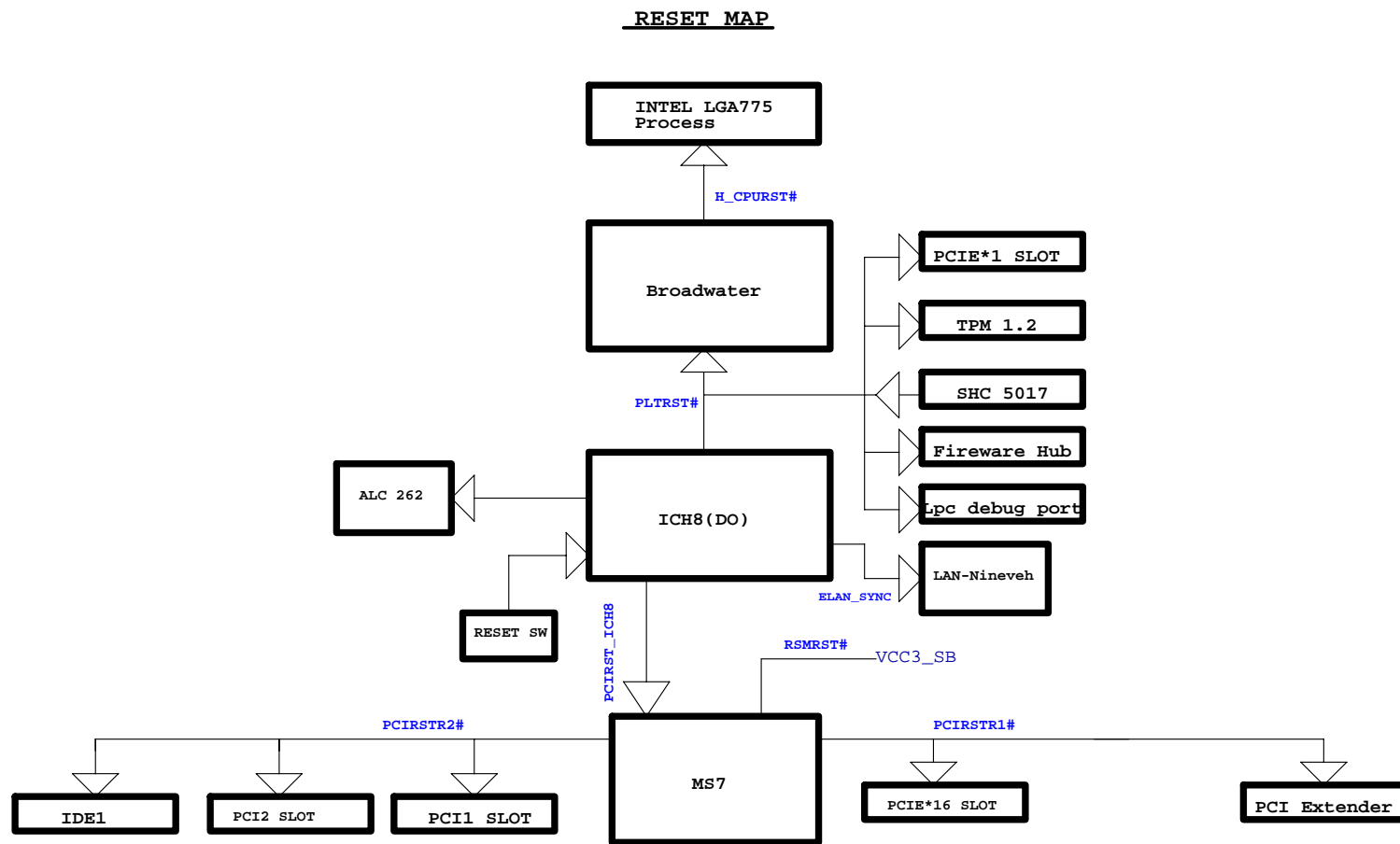
JUMPER SETTING

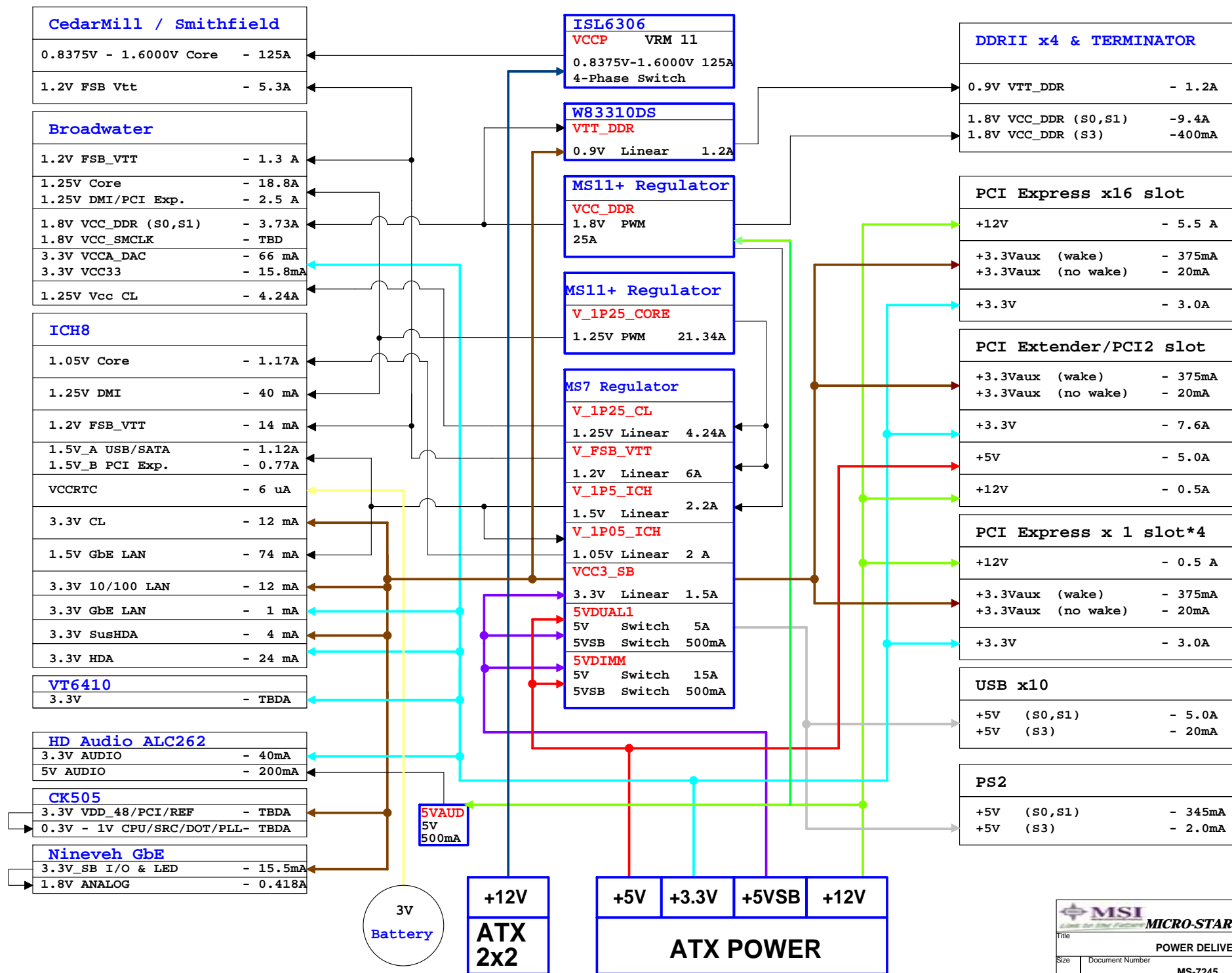
JBAT1	(1-2)Normal	(2-3)Clear
INTRUDER	Short Normal	Open warning
JPWD1	(1-2) open clear	(1-2)short Normal

 MICRO-START INTL CO.,LTD.		
Title		
GPIO PIN definition		
Size	Document Number	Rev
	MS-7245	1.0
Date:	Monday, September 04, 2006	Sheet 31 of 35

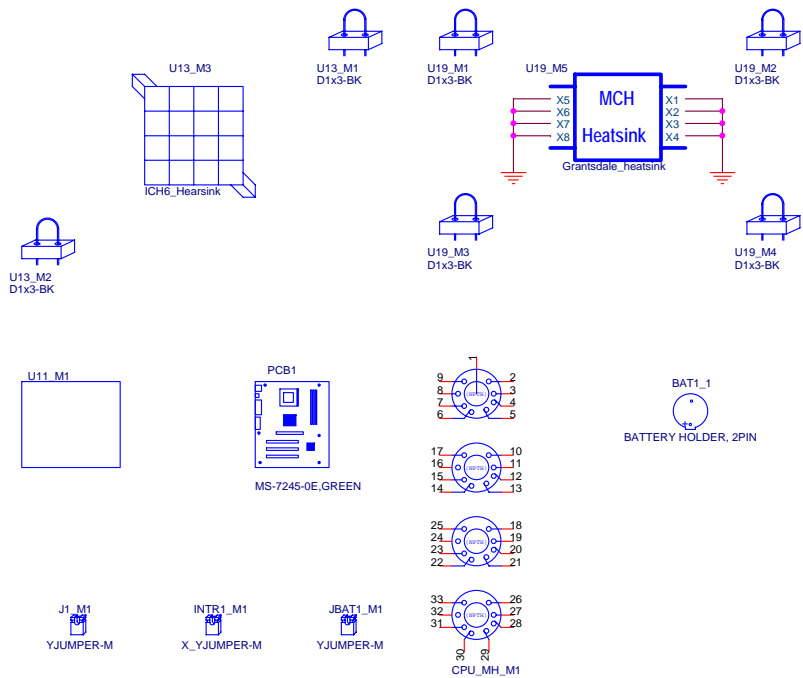
PWROK MAP







COMMON MANUAL PART



MT3H MANUAL PART

